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PULSED GAAS IMPATT DIODE DEVELOPMENT.(U)
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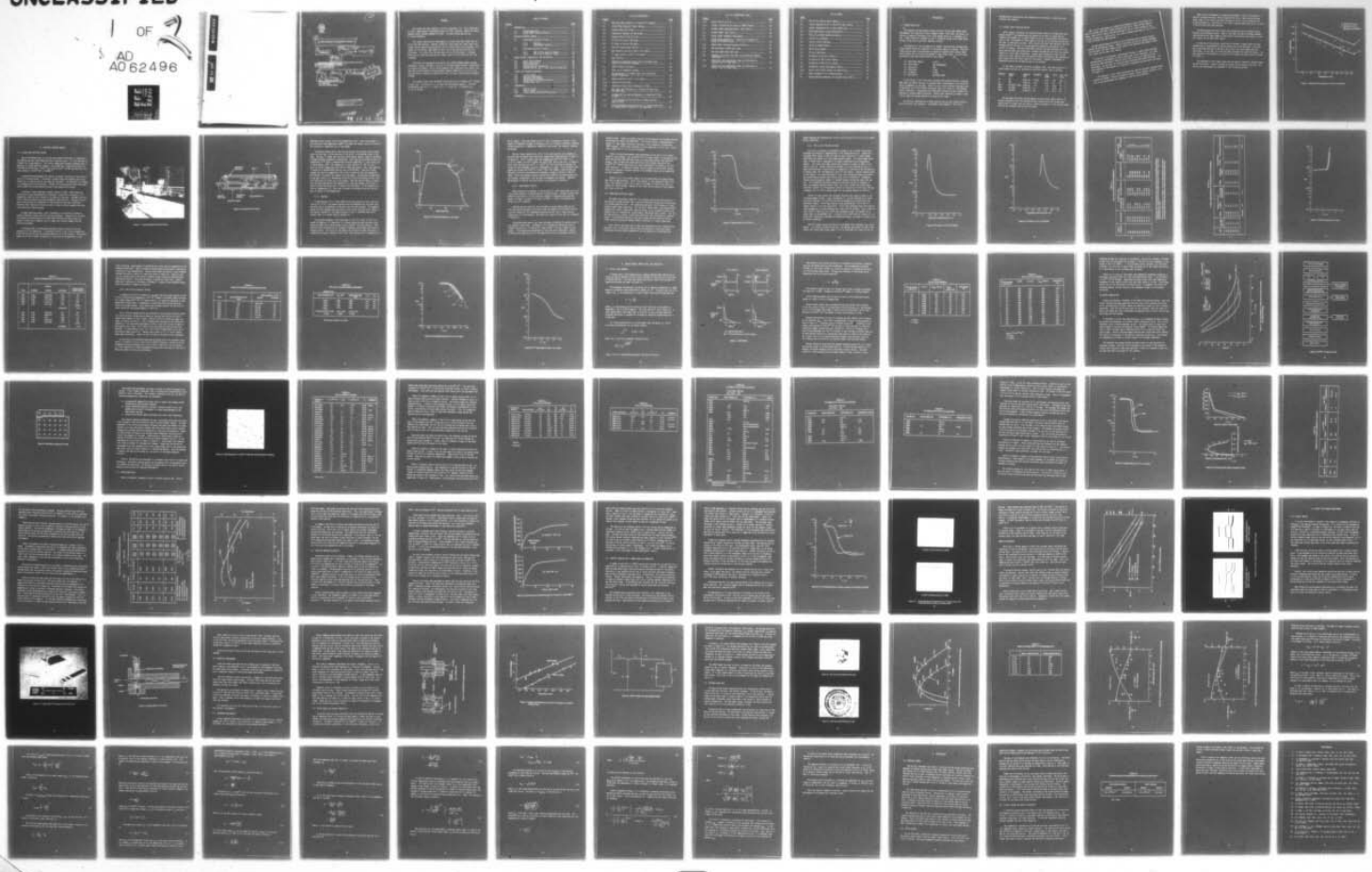

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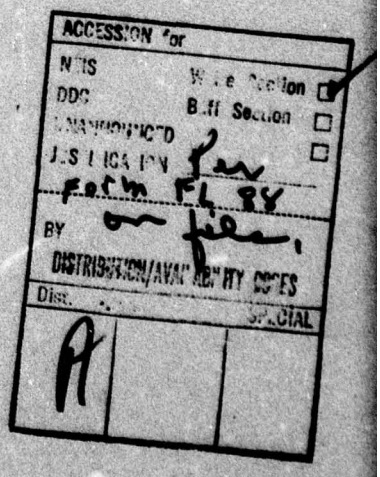
FOREWORD

This report has been prepared by Varian Associates, Inc., Solid State West Division, Semiconductor Engineering Group as a final technical report for Naval Weapons Center Contract N00123-76-C-1063. The NWC program monitor was Mr. Marko Afendykiw.

This report describes the development of Ku-band GaAs Read Impatt devices for pulsed applications. Material growth by liquid phase and vapor phase techniques, device design and evaluation, and rf-circuit design are discussed. As a result of this effort, peak power of 20.5 W at 13 GHz was achieved with 21% efficiency. At 14 GHz, 16 W was obtained with 19.1% efficiency. A maximum efficiency of 23.6% was obtained at a power level of 8.25 W peak for the same frequency.

The effort was sponsored by the NAVAL SEA SYSTEMS COMMAND Combat Systems Development Branch (SEA-0324), the Naval Air System Command Weapons System Analysis Branch (AIR-03P24), the Air Force Armament Test Laboratory (AFATL/DLMI) and the Army Missile Research and Development Command (DRDMI-CD) as a part of the TRI-Service-Fast Acquisition Search and Track (Tri-Fast) Technology Development Program.

This report covers work performed during the period 1 November 1976 through 31 July 1977. At Varian, Dr. F. B. Fank was the program manager. Principal investigators were Mr. T. L. Hierl, Dr. S. I. Long, Mr. J. Kinoshita and Dr. B. R. Cairns.



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1. INTRODUCTION

1.1 PROGRAM OBJECTIVES

The research and development program entitled "Pulsed GaAs IMPATT Diode Development" was sponsored by Naval Weapons Center, China Lake, California, to provide an improved high-power solid state pulsed source at a frequency of 14 GHz. These diodes are intended for use in injection-locked solid state transmitters using cavity-type power combiner circuits.

The objective of this program was to design, fabricate and evaluate GaAs pulsed IMPATT diodes for generation of microwave energy in Ku-band. High efficiency devices were to be designed to operate at moderate duty cycles, short pulse lengths and to provide the maximum in peak output power. The following performance goals were established for this effort:

(a)	Peak Power Output	$\geq$ 20 W
(b)	Pulse Width	125 nanoseconds
(c)	Duty Cycle	10%
(d)	Efficiency	$\geq$ 20%
(e)	Frequency	14 GHz
(f)	Reliability	300 Hours MTBF

As the intent of this study was to advance the state-of-the-art in pulsed GaAs Read type IMPATT devices, an approach which investigated a wide variety of device parameters was selected. Both hi-lo and lo-hi-lo device structures were investigated in parallel efforts using both grown (p^+) junctions and Schottky barrier junctions. Liquid-phase and vapor-phase epitaxial growth methods were employed to produce these structures. Efforts were conducted to create a theoretical model for pulsed operation of these device types.

Reliability investigation of grown junction devices and various Schottky barrier material was conducted. Considerable improvements in the circuit

package-device interactions were completed which resulted in significant performance improvements.

1.2 PULSED IMPATT STATE-OF-THE-ART

While several high-power and high-efficiency results on CW GaAs Read type Impatt diodes[1,2] had demonstrated the capability of GaAs to exceed the performance achievements of Si Impatt diodes by virtue of much higher efficiencies (35% vs 15%), development of these types of devices for pulsed applications had not been as extensively pursued. Early results obtained from operating these CW Schottky barrier devices in a pulsed mode were generally unsuccessful for a variety of reasons. Much more encouraging results had been achieved utilizing grown junction GaAs Read structures; although the majority of effort was concentrated at C- and X-band frequencies. Output powers competitive with silicon double drift (DD) devices with considerably higher efficiencies were reported on GaAs single drift (SD) grown junction structures.[3] However, development of comparable devices for Ku-band had yet to be explored.

At the time of program initiation (November 1976), the state-of-the-art in pulsed Impatt devices, as reflected by published reports, was as follows:

MATERIAL	DEVICE TYPE	JUNCTION TYPE	FREQUENCY	PEAK POWER	EFFIC.	DUTY CYCLE	REF
Si	DD	Grown pn	10 GHz	18 W	12%	25%	4
Si	DD	Grown pn	16.5	13.5	12	25	4
GaAs	DD Hybrid Read	Grown pn	5.8	4.4	22.5	25	3
GaAs	SD Read	Grown p^+n	10	8.0	26.8	25	3
GaAs	SD Read	Grown p^+n	10	17.3	21.3	25	5

Varian began the design and development of GaAs pulsed Impatt devices for Ku-band frequencies with the expectation that designs which had already been established for X-band could be readily scaled to operate at 14 GHz on both grown junction and Schottky barrier junction types.

Some initial development of 14-GHz devices began in March 1976 funded in a parallel program from AFAL, Wright Patterson AFB, Ohio. When the NWC program began, some initial results had been obtained on the Air Force program at low Ku-band frequencies. Specifically, at 14 GHz a maximum peak power of 10.7 W with 17.5% efficiency had been obtained.

The NWC program began building on this technology base to advance device designs and performance levels. Many of the tasks carried out between November 1976 and March 1977 were common to both efforts and therefore may appear in both this report and the AFAL final report.

At the end of the program, considerable increase in power output had been achieved due to improvements in device design and circuit matching. At 13 GHz, 20.5 W had been obtained at 10% duty cycle, 500 n sec pulse length with 21% efficiency. At 15.4 GHz, 15 W had also been achieved with 18.3% efficiency. The best observed rf performance as a function of frequency and duty cycle are shown in Figure 1.1.

The remainder of this report describes the specific technical approach taken during this effort. Details on material growth, device designs, junction, reliability and performance are presented in the following sections.

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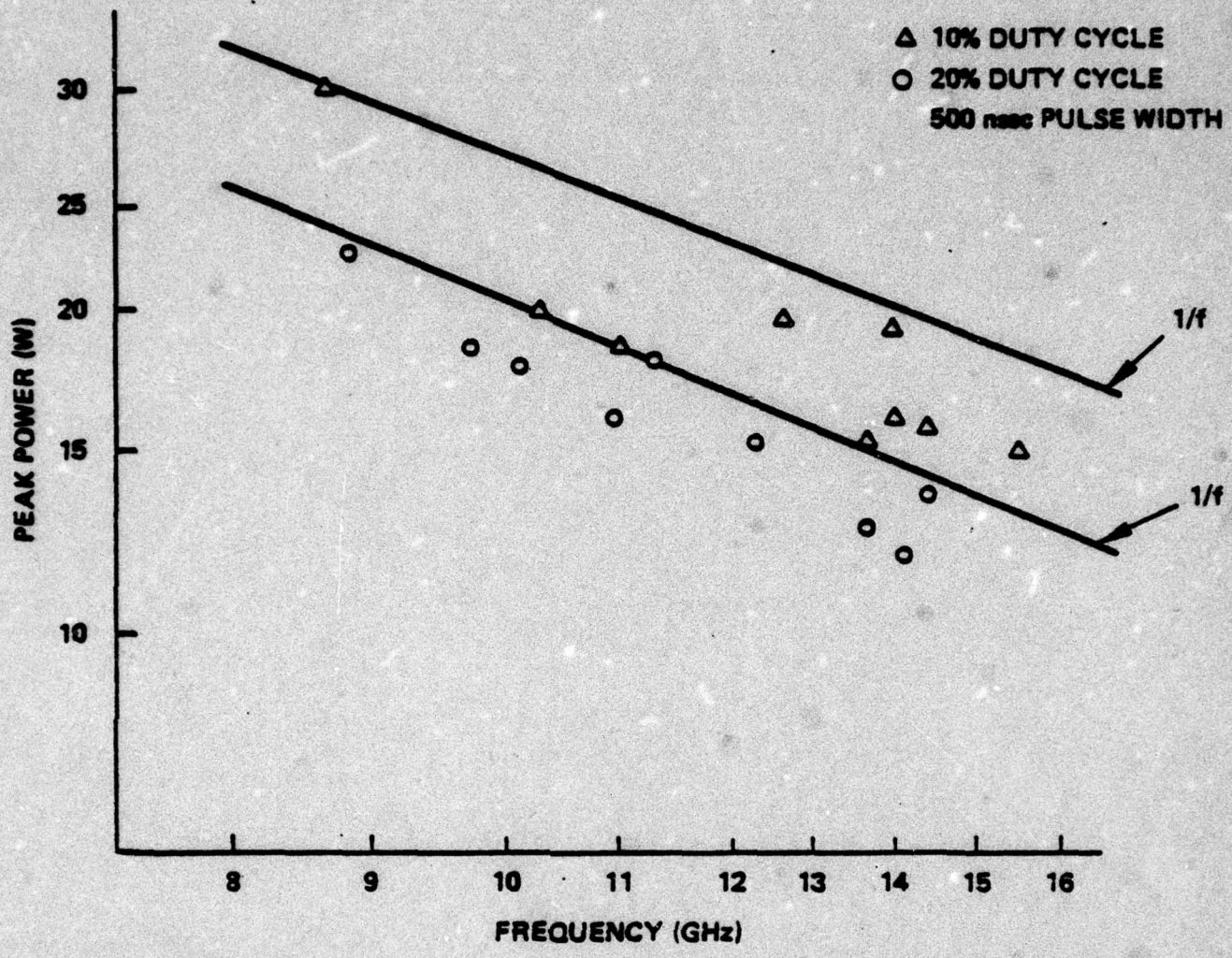


Figure 1.1 Best Peak Power Results as a Function of Frequency

2. EPITAXIAL MATERIAL GROWTH

2.1 LIQUID-PHASE EPITAXIAL GROWTH

One of the methods used to grow the multilayered structures as required for the IMPATTs was the liquid-phase epitaxial technique (LPE). Tin (Sn) was used as a dopant for n-type material. The lightly compensated acceptor germanium (Ge) is employed for p-type epitaxial growth. Each dopant has a characteristically low distribution coefficient (7.9×10^{-5} for Sn and 8.3×10^{-3} for Ge) and both have low vapor pressure ($\sim 7 \times 10^{-8}$ Torr at $1000^{\circ}K$)[6].

A standard Varian-designed LPE reactor (as shown in Figure 2.1) was used for the p^{+}-hi-lo wafer growth. A three-well graphite boat with moveable wells (see Figure 2.2) is used to contain two doped gallium melts. The substrate is located in a recessed slot below the melts. Contact with and extraction from either melt can be controlled by positioning the wells from outside the furnace.

A clam-shell type three-zone Lindberg furnace is used. These zones are controlled by three Leeds-Northrup "Electromax" controllers to maintain $\pm 1^{\circ}C$ temperature stability and flatness in the region of the boat. Hydrogen purification is being performed by palladium membrane type purifiers. Hydrogen line and quartz reactor parts are assembled to high vacuum He leak-tight conditions. Stainless steel tubing and valves are used in order to assure oxygen-free conditions within the reactor system.

Sn doped substrate wafers, (100) orientation, are carefully polished by chemical mechanical means using the Br_2-CH_3 OH method. Preparation of the wafer for epitaxial growth consists of a multi-step cleansing procedure employing organic solvents and a chemical etch to remove any residual damage from the polishing procedure.

A transient mode of liquid-phase epitaxial growth is used for gallium arsenide thin film deposition. A saturated solution of As in Ga is prepared by dissolving high purity gallium arsenide dendrites in a gallium melt. The desired dopant (Sn or Ge) is added to the melt to bring carrier concentration in the

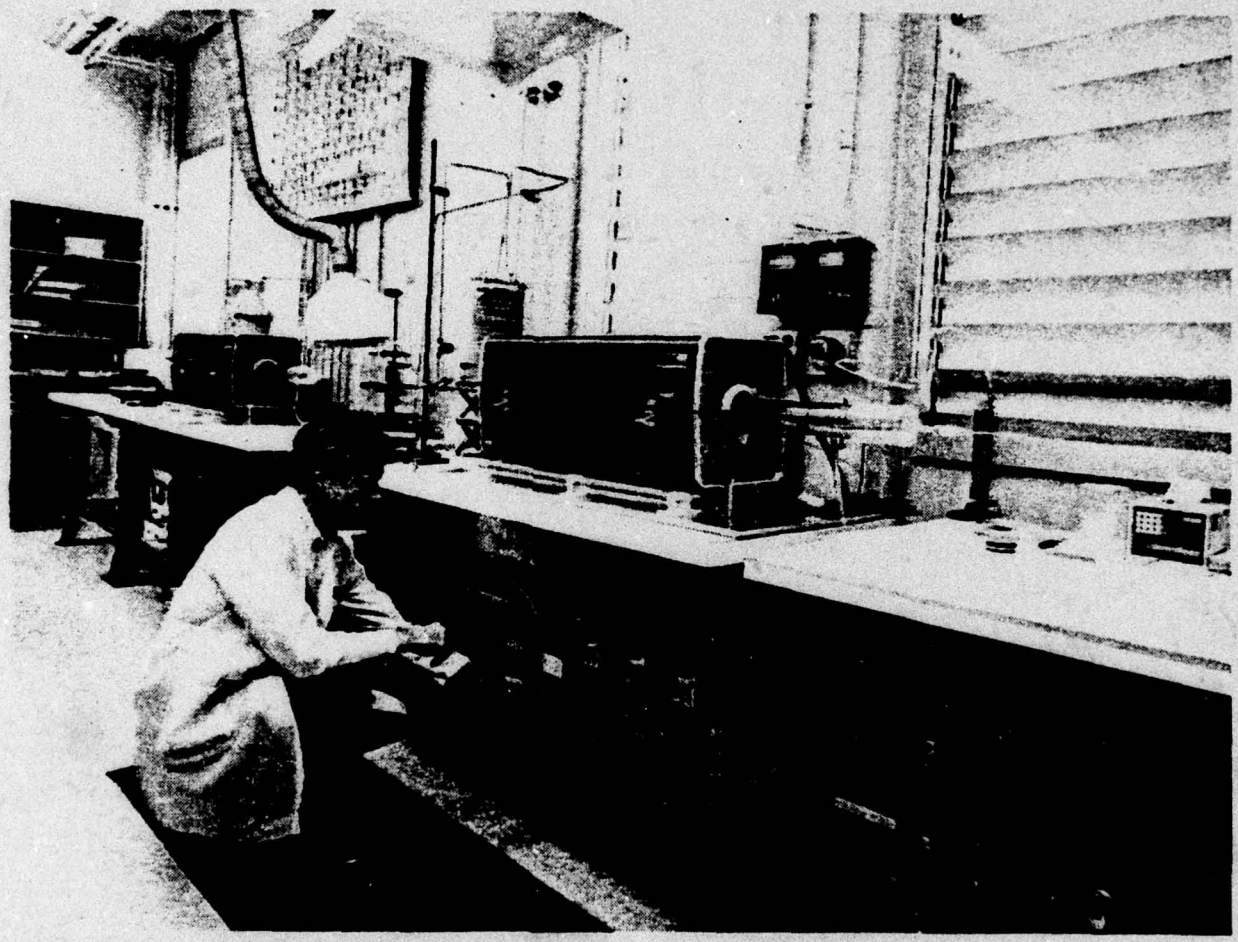


Figure 2.1. Liquid Phase Epitaxial Growth System

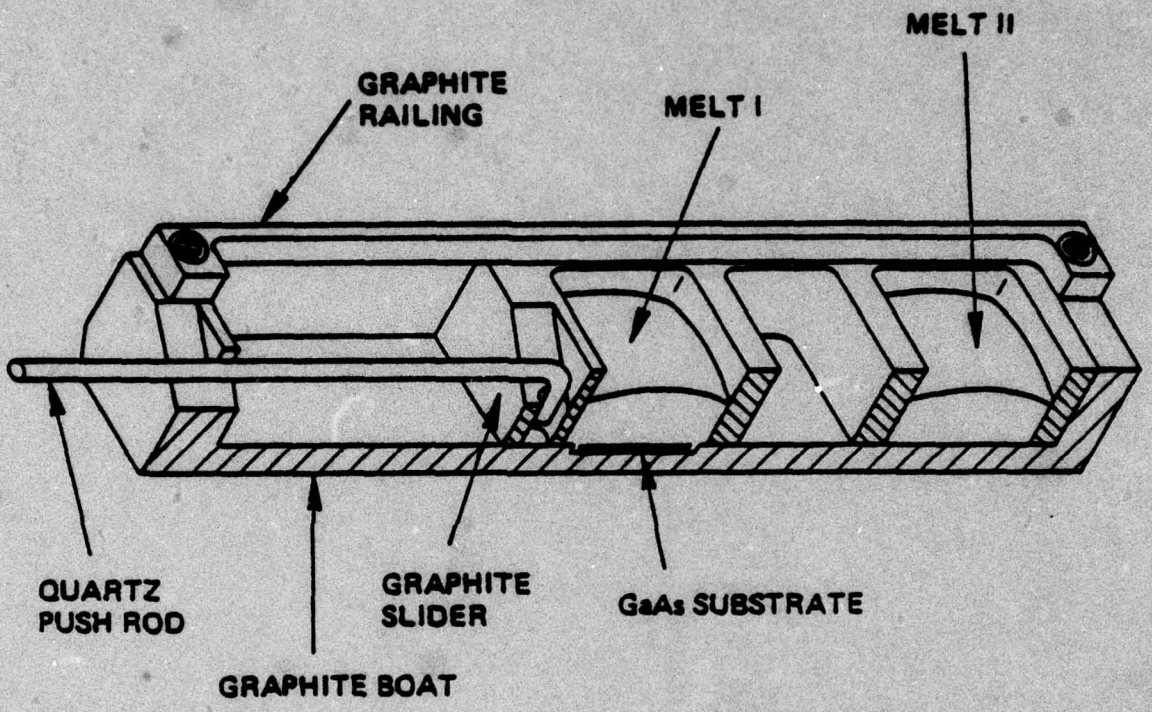


Figure 2.2 Graphite Boat with Slider

deposited single crystal film to the appropriate level. Melts are brought to equilibrium at high temperature (900°C) and baked for several hours to allow for the diffusion of impurities out of the system.

The growth process starts with placing the gallium arsenide single crystal wafer (3.5 cm long, 1.25 cm wide and 0.3 cm thick) in the bottom recess of the boat. The boat is loaded into the high purity quartz reactor, where a palladium-diffused hydrogen atmosphere is maintained. After heating the graphite boat to a temperature of 5° above a predetermined starting temperature T_1 (see Figure 2.3) of approximately 705°C, the temperature is kept constant for half an hour in order to achieve temperature equilibrium within the system. Then, the apparatus is cooled at a predetermined cooling rate (0.5°-2°C/min). When the furnace reaches the starting temperature, the slider is moved so that the appropriate gallium melt is brought into contact with the wafer. The decreasing temperature of the melt results in a decreasing solubility of gallium arsenide solute, thus solid GaAs must be frozen out of the system. When the desired amount of deposition has been obtained and the temperature T_2 has been reached, the slider is moved to bring the second melt in contact with the wafer. At the completion of the run (temperature T_3), the slider is moved to the neutral position and the boat is cooled to room temperature.

2.1.1 Approach

As the complete p^+-hi-lo Read IMPATT structure consists of four epitaxial films (p^+-n^+-n^--n^+), the growth sequence must be separated into two runs; only two melts can be accomodated in the boats used for this program. The sequence chosen for this purpose required growth of the buffer layer and drift region in one reactor (system "R") followed by growth of the n^+ avalanche zone and p^+ contact layer in a second reactor (system "C").

An alternate sequence, involving growth of the n^+-n layers in the first system followed by a p^+ deposition in a second system had been previously evaluated and found to be unsatisfactory due to junction interface defects. These junctions were characterized by premature breakdown, microplasmas and excessive leakage current. The cause for the defects has tentatively been attributed to insufficient surface cleaning of the n^+ epi layer surface prior to deposition of

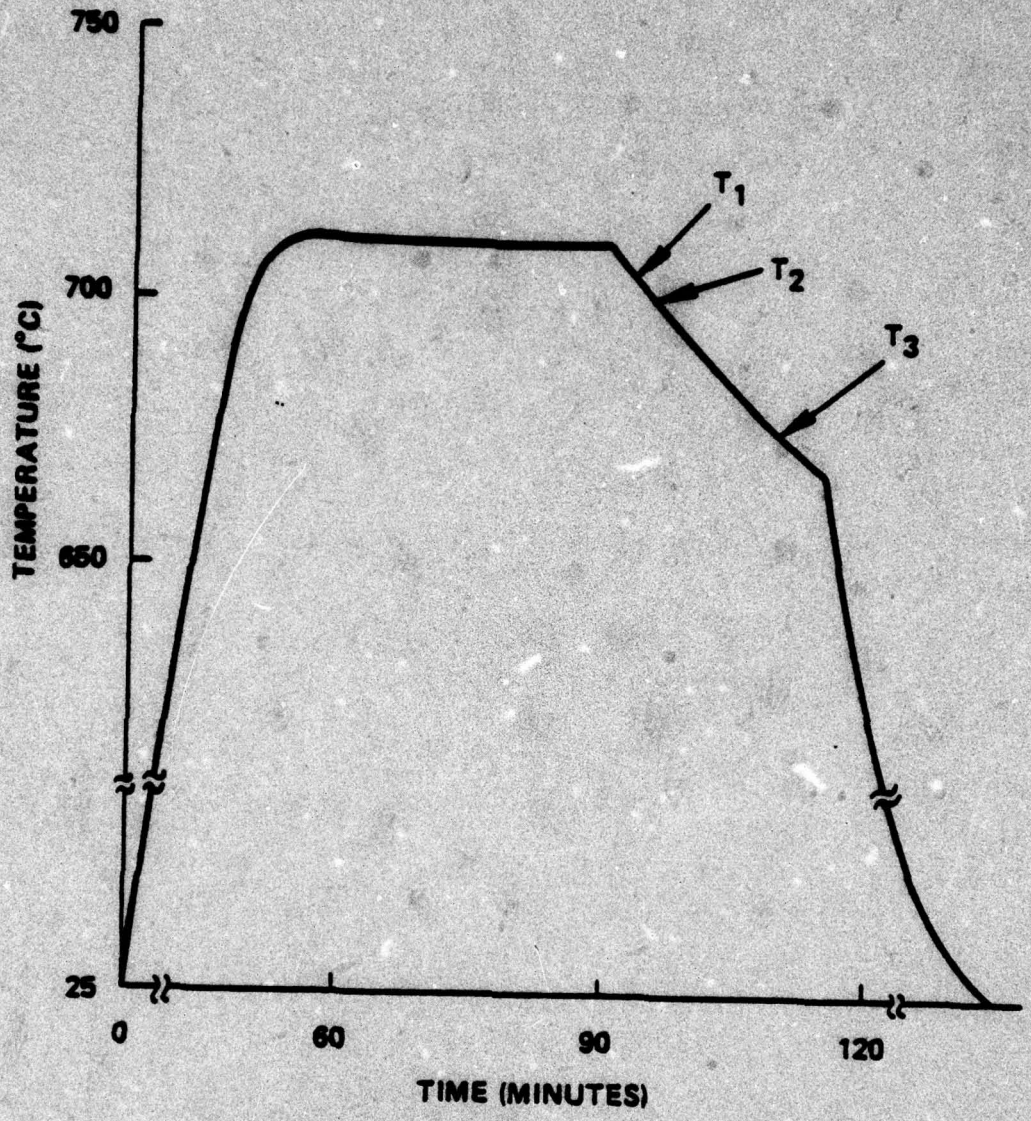


Figure 2.3 Temperature Schedule for LPE Growth

the p^+ region. Since the length of the n^+ layer is extremely critical in the control of breakdown voltage, no etching prior to p^+ growth is possible. Adequate surface preparation is apparently impossible using normal wet chemical cleaning techniques.

The four layers deposited for the p^+ hi-lo device wafers were targeted at the drift and avalanche layer doping and length specifications shown in Table 3.1 in Section 3. The p^+ contact layer was targeted at $1x10^{18}$ cm^{-3} and 1.0 to 1.5 μm in length, and the n^+ buffer was $5x10^{17}$ cm^{-3} and 2-3 μm long. A range of drift layer dopings from $4x10^{15}$ to $1.2x10^{16}$ cm^{-3} was evaluated to explore the effects of this parameter on device performance at 14 GHz. Also, avalanche zone doping was varied from $4x10^{16}$ to $1.2x10^{17}$ while the length at each doping was adjusted to provide room temperature breakdown voltage in the 25- to 35-volt range. While the complete range of combinations possible for these dopings was not covered, a meaningful cross section of parameters was sampled. Measured performances of devices from these wafers are presented in Section 4.

2.1.2. Experimental Results

Wafers grown by the approach in which the p^+-n^+ layers were grown on an n-n^+ drift region generally exhibited good dc characteristics. Leakage currents were generally less than 0.1 μA and life-test studies on these devices projected median lifetimes in excess of 10^3 hours at 300°C. A total of 26 wafers were grown using this approach.

Schottky barrier junctions were evaluated on three wafers grown by LPE. This was possible because part of each wafer was masked from p^+ deposition and could be cleaved off for independent Schottky barrier and p^+ grown junction comparisons of rf performance. The electrical results of the runs are discussed in Section 3.

Evaluations were made of epi layer thickness uniformity for wafers grown in the standard slider boat. Thickness of n^+-n growths was controlled within a standard deviation of ± 12.8% and p^+ layers within ± 7.7% on a sample of ten wafers. Thicknesses were determined by cleave and stain techniques. Doping uniformity was excellent for all LPE depositions with no detectable variation

across a wafer. Figure 2.4 shows a doping profile measured from Schottky barrier capacitance for wafer E 551/C677/R631. This profile gives a representation of typical n^+ layer length uniformity achieved in this system for Ku-band Read IMPATT growths. Drift layer thickness for this wafer was 3.9 to 4.4 μm. The p^+ layer ranged from 1.4 to 1.8 μm in thickness.

Yields to device performance were determined for the LPE p^+ hi-lo wafers grown for this program. Out of the 26 p^+ hi-lo wafers grown, six yielded devices which gave greater than 20% efficiency, and eight gave greater than 15% efficiency. This includes five wafers which had drift regions outside of the $5\text{-}8\text{x}10^{15}$ cm^{-3} doping range which was later determined to be necessary for efficient operation. If these are deleted from the sample as being drift regions known to be purposely selected outside of the optimum range, yields become 29% and 38% respectively.

Growth of $n\text{-}n^+$ drift-buffer layers can be accomplished with approximately 90% yield to specification. The p^+ layer growth is also successful 90% of the time. The remaining yield loss is due to the degree of control over the avalanche (n^+) region length. Doping of this layer can be controlled very repeatably from run to run.

2.2 VAPOR-PHASE EPITAXIAL GROWTH

The IMPATT structures needed for this program required precise control of the epitaxial growth process, and it was also desirable to grow entire structures in a single deposition run. The vapor-phase epitaxial (VPE) process is a good choice to meet these conditions. For this work, Varian used a new electronically operated VPE reactor system which used the $AsCl_3$, Ga, H_2 transport process with capabilities of n-type doping, p-type doping, and excess $AsCl_3$ control. Gas flow was controlled by a system of mass flow controllers and electronically operated valves. This minimized operator error and allowed precise timing of the gas flows required to grow the complex IMPATT structures in a single deposition.

After initial runs were made to show that background carrier concentrations and mobilities vs $AsCl_3$ mole fraction were as expected for high purity GaAs, calibration runs were begun immediately with the objective of optimizing the

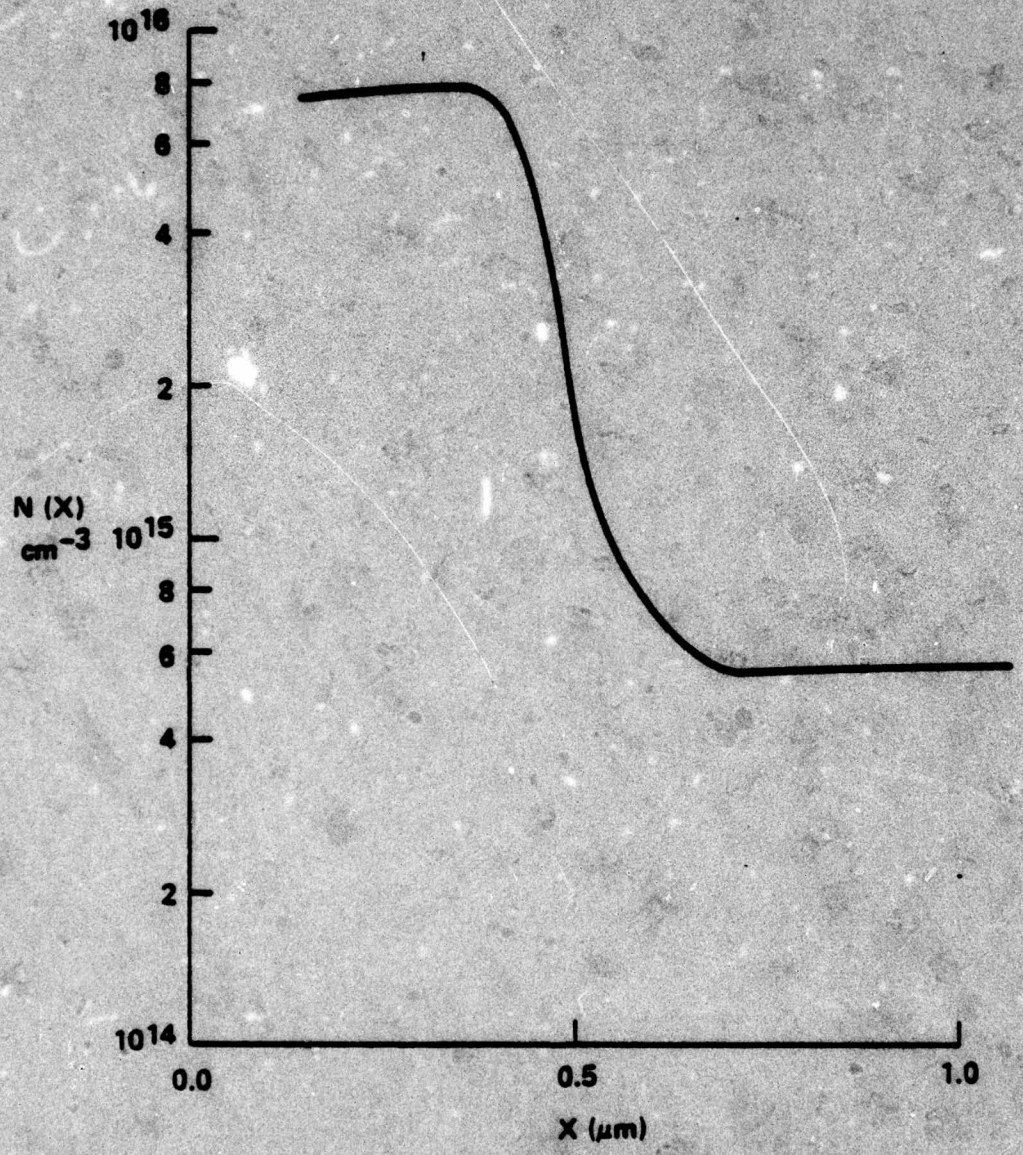


Figure 2.4 Doping Profile of LPE p^+ Hi-Lo

growth sequence and processes for lo-hi-lo (n-n^+-n) and p^+-hi-lo (p^+-n^+-n) IMPATT device structures.

2.2.1 VPE Lo-Hi-Lo Material Growth

The lo-hi-lo structure is preceded by growth of an n^+ buffer layer which minimizes the effects of imperfections in the substrate material. Growth of a low doped drift region is then followed by rapid injection of a highly doped spike layer and growth of a lower doped contact region. The highly doped spike layer is grown using a combination of dopant concentration and backpressure control. This gives very sharp spikes with narrow half-width as shown in Figures 2.5 and 2.6. Abrupt transitions between layers are effected by use of a vapor etch technique in which growth is temporarily inhibited by the introduction of excess $AsCl_3$ into the deposition region of the reactor. Doping concentrations in the reactor are re-equilibrated at a new level during the vapor etch period and growth begins abruptly when excess $AsCl_3$ flow is terminated. Autodoping effects are minimized by removal of residual dopants during the vapor etch period. This technique eliminates mechanical coupling required to transport a substrate between multiple growth zones, and is well suited for either manual electronic control or microprocessor control of production of multilayer devices. A summary list of lo-hi-lo wafers grown for the program appears in Table 2.1.

Control of layer doping and thickness has been quite good as shown in the following summary tables. Layer thicknesses of 1 μm were obtained by a cleave and stain technique. C-V profiles provided thicknesses and doping levels for sub-micron layers. Drift layer doping varied approximately ± 4% to 5% in a typical series of six runs (Table 2.2). Drift layer thickness must fall within a range bounded by a critical minimum and a less critical maximum. Four of the six runs listed in Table 2.2 fall within the acceptable range, and another falls quite close to the maximum limit. A typical drift layer profile (Figure 2.7) is quite flat, indicating a minimum of autodoping effects, and shows an abrupt drift to buffer transition.

Table 2.3 shows run-to-run control in avalanche layer thickness (i.e. spike depth). In a typical series of ten runs, the average spike depth for 80% of the wafers fell within 15% of the target. This is quite good for layers as thin as

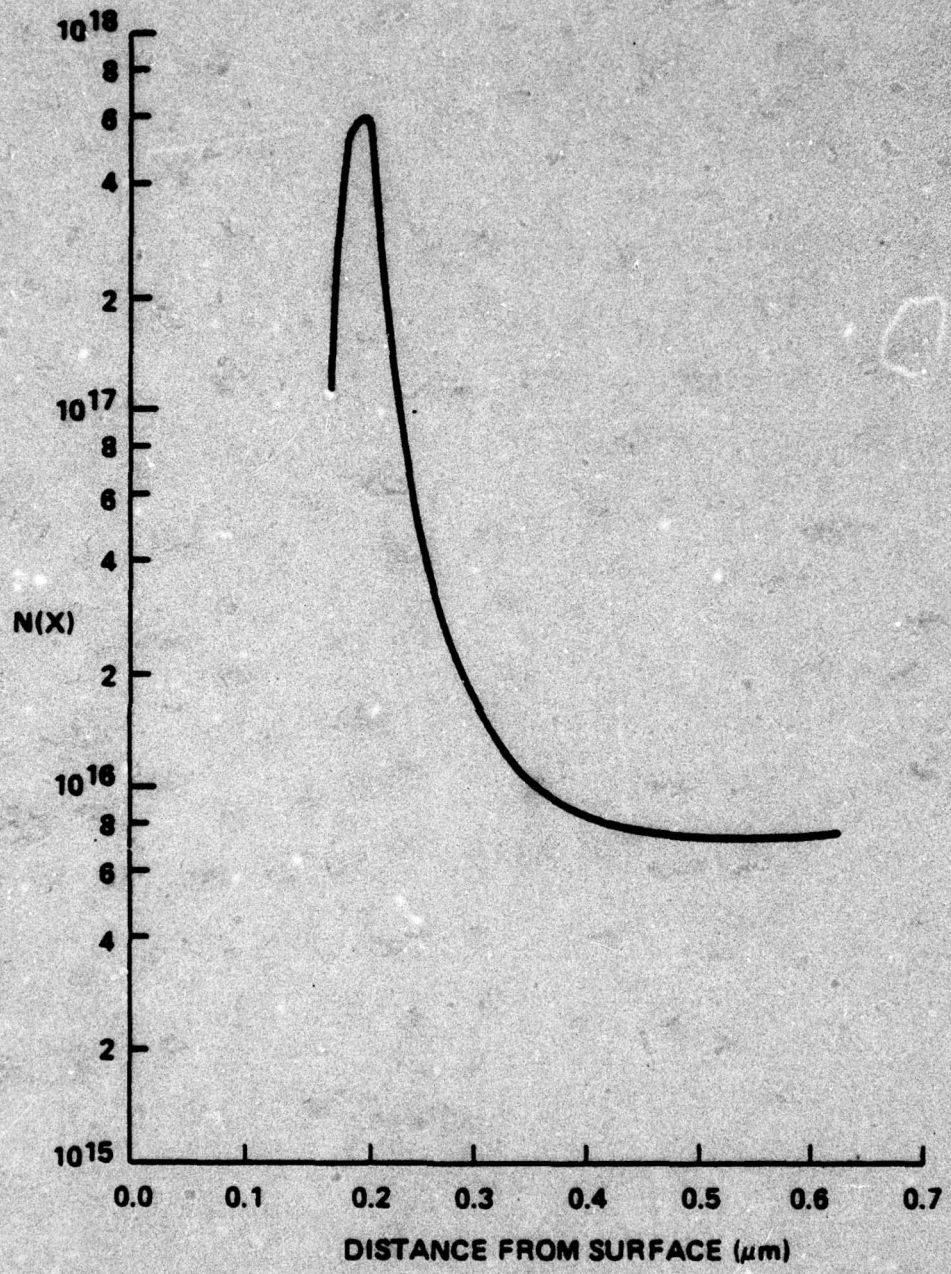


Figure 2.5 N^+ Spike of Lo-Hi-Lo VPE Wafer

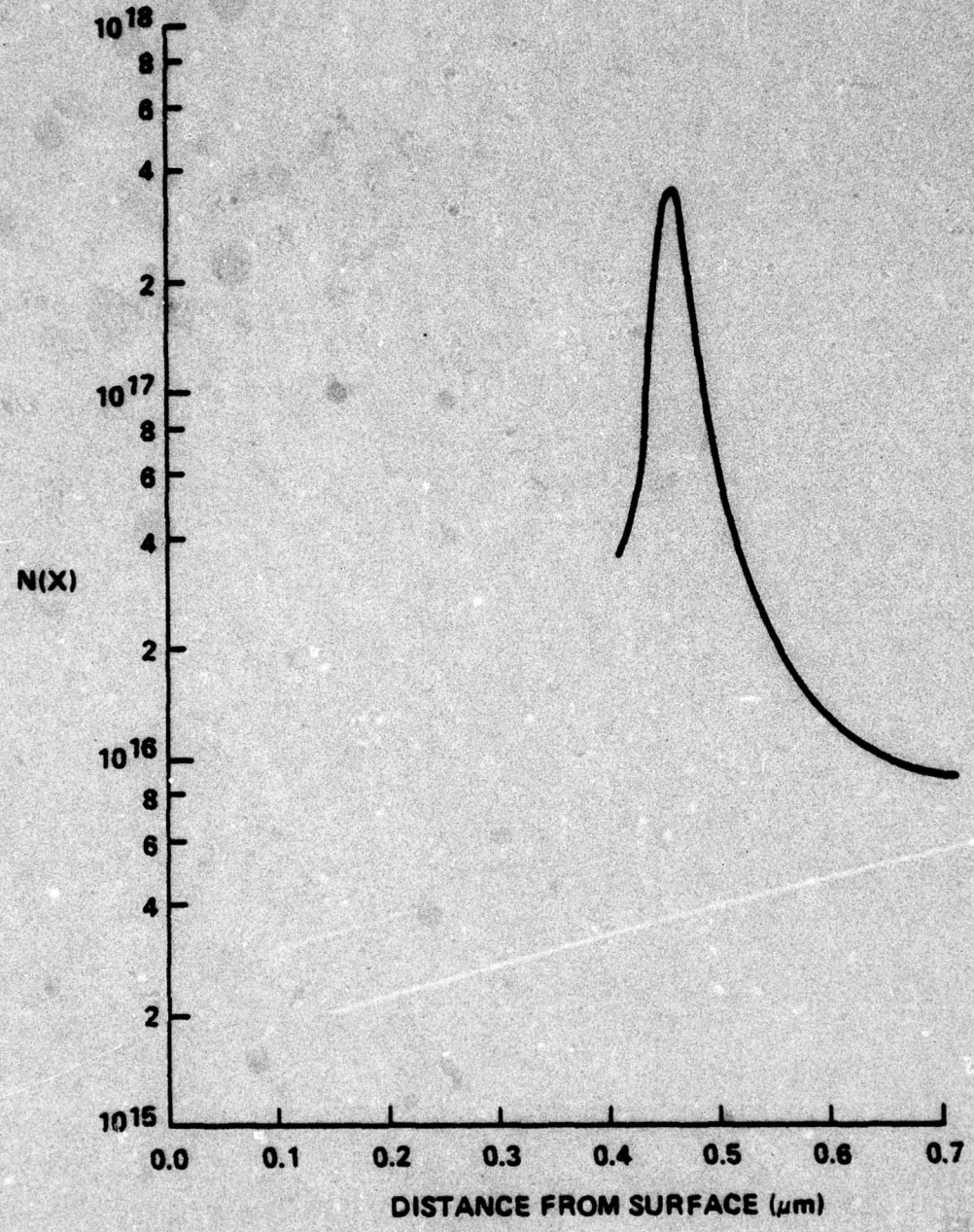


Figure 2.6 N^+ Spike of Lo-Hi-Lo VPE Wafer

TABLE 2.1
VPE LO-HI-LO DEVICE WAFER SUMMARY.

DEVICE E RUN NO.	EPI RUN NO.	HI SPIKE LAYER PEAK DOPING $N \times 10^{17}\ cm^{-3}$	HI SPIKE LAYER PEAK DEPTH (μm)	WIDTH ½ MAX. (Å)	DRIFT LAYER DOPING $N \times 10^{15}\ cm^{-3}$	DRIFT LAYER WIDTH (μm)
417	A2–9B[+]	2.5–2.6	0.54–0.57	500	13–13.5	4.2
436	A2–4A	3.6–3.7	0.31–0.35	600–630	6.0–6.2	3.35
460	A4–8A	2.4	0.49–0.53	480–500	8.0–9.0	5.35
480	A5–4A[+]	3.7–3.8	0.46	350–400	10.0	5.78
487	A6–4A	3.9–4.0	0.23–0.24	450–500	8.0–8.6	4.1
524	A6–6A[+]	5.0–5.2	0.17–0.20	350–400	7.2–7.8	3.6
525	A6–6A[+]	8.0	0.175	450	7.0	5.0
526	A6–7A	7.5–9.0	0.21–0.24	400–450	7.0–7.6	3.91
544	A7–8A	7.4–7.5	0.40–0.43	500	10.0	5.57
545	A8–3A	5.5–6.0	0.20–0.23	350–400	7.8–8.5	3.04

+ Wafers from some runs were cleaved into multiple sections to receive different thinnings, metallizations, etc. Each section has been assigned a separate E number. Device testing data is listed by E number.

* This data was obtained from C-V profiles of "as grown" epitaxial wafers. Final profiles from a device (after thinning and processing a wafer) will yield slightly different data.

TABLE 2.2
TYPICAL REPRODUCIBILITY IN VPE DRIFT LAYER DOPING

RUN	H_2S CONC. ppm x 10^2	DOPING n x 10^{15} cm^{-3}			THICKNESS (μm)			
		RANGE	AVERAGE	% DEVIATION FROM AVERAGE	TARGET	ACCEPTABLE RANGE	ACTUAL	% DEVIATION FROM TARGET
A6-2	5.4	7.7–8.0	7.9	0.6	5.0	4.0–5.0	4.6	8.0
A6-3	5.4	8.1–8.2	8.2	4.5	4.0	4.0–5.0	5.7	42.5
A6-4	5.4	8.1–8.6	8.4	7.0	3.5	3.0–4.0	4.1	17.1
A6-5	5.4	7.2–7.8	7.5	4.5	3.5	3.0–4.0	3.6	2.9
A6-6	5.4	7.3–7.8	7.6	3.2	3.25	3.0–4.0	3.6	10.8
A6-7	5.4	7.0–7.6	7.5	4.5	3.5	3.0–4.0	3.9	11.4
		AVERAGE	7.85	4.1%				16.6%

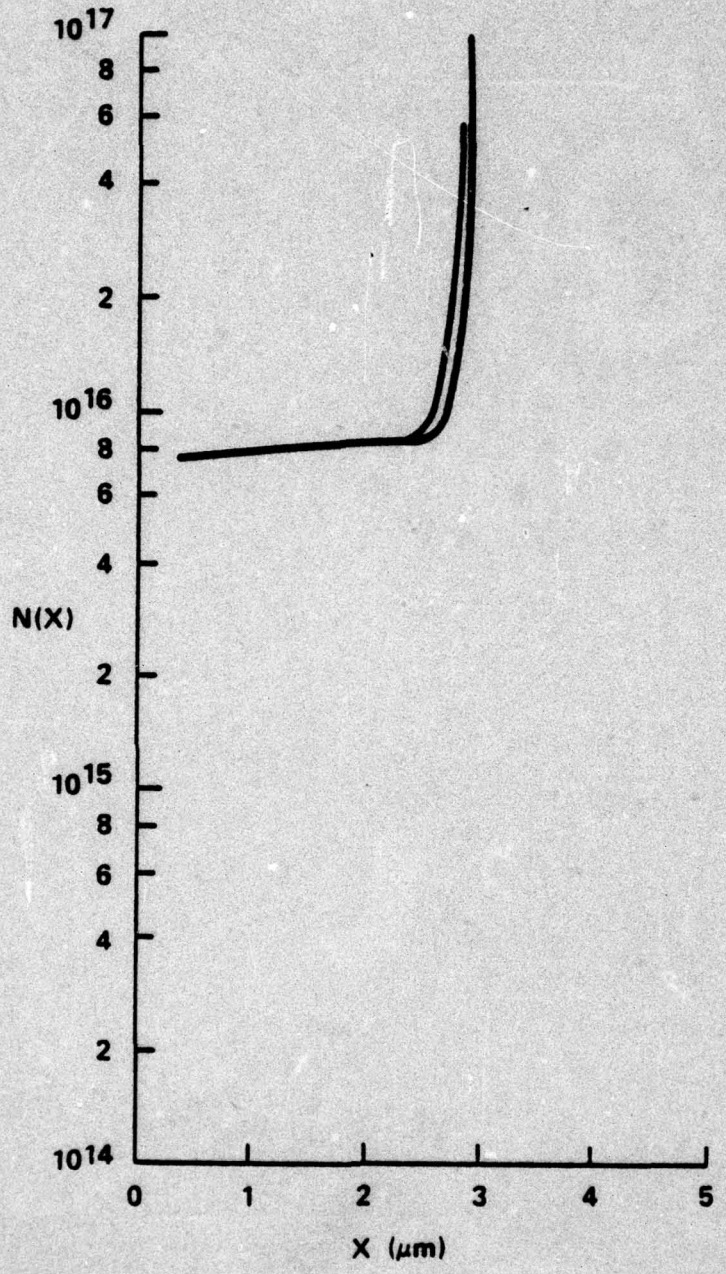


Figure 2.7 VPE Drift Buffer Layer Profile

TABLE 2.3
TYPICAL REPRODUCIBILITY IN SPIKE DEPTH (μm)

RUN	TARGET	ACTUAL RANGE	AVERAGE	% DEVIATION FROM TARGET
A6-2	0.25	0.23–0.25	0.24	4.0
A6-4	0.225	0.23–0.24	0.24	6.7
A6-5	0.20	0.17–0.20	0.19	5.0
A6-6	0.20	0.16–0.19	0.17	15.0
A6-7	0.20	0.21–0.24	0.22	10.0
			AVERAGE	8.1%
A5-2	0.45	0.38–0.42	0.41	8.9
A5-3	0.45	0.39–0.40	0.39	13.3
A5-4	0.45	0.46	0.46	2.2
A5-6	0.35	0.38–0.39	0.38	8.6
A5-7	0.35	0.33–0.36	0.34	2.9
			AVERAGE	7.2%

0.20 to 0.45 μm. Spike doping is controlled by varying the H_2S concentration and injection conditions. Table 2.4 shows very good spike doping control obtained as a function of H_2S concentration. Typical spike depth and doping Q, and breakdown voltage from point to point on a wafer are given in Table 2.5. Tables 2.4 and 2.5 also contain data on the typical spread of spike doping and depth obtained from several wafers. Very good uniformity is shown for these runs. Typical spike half widths are on the order of 350-500 Å. Spikes of two different doping levels are shown in Figures 2.5 and 2.6.

2.2.2 VPE p^+-Hi-Lo Material Growth

In growth of the p^+-hi-lo material, the spike and the contact regions of the lo-hi-lo structure are replaced by a 10^{17} cm^{-3} doped n^+ avalanche region followed by a highly doped $4x10^{17}$ cm^{-3} p^+ contact region. No injection technique is used. Deposition of each layer is preceded by a vapor etch period during which gas flows are re-equilibrated. Layer doping and thickness control for the p^+-hi-lo wafers grown for the program appears in Table 3.5.

The p^+ carrier concentrations were obtained by calculations using net effective profiles which include the as-grown p/n junction and profiles of the n^+ region after removal of the p^+ layer. Typical profiles of these two types are shown in Figures 2.8 and 2.9. The p^+ concentration obtained by this method was compared to a dc resistance measurement of the p^+ layer which gives an approximate doping level value. Half widths of the net effective profiles were also measured. At these doping levels, an n^+ half width of 2600 Å gave V_B values in the desired range (Table 3.5). Doping level control of p^+, n^+, and n regions shows good consistency. Control of the n^+ width is the most critical parameter.

In conclusion, VPE processes have been developed which give reasonably good control in growth of lo-hi-lo and p^+-hi-lo IMPATT structures. The most critical parameters are the spike depth for lo-hi-lo and n^+ width for p^+-hi-lo material. V_B is very sensitive to these thicknesses and many more runs would be required to determine yields to device specifications.

TABLE 2.4
SPIKE PEAK DOPING vs H_2S CONCENTRATION

RUN	H_2S CONCENTRATION (ppm)	PEAK DOPING n x 10^{17} RANGE	AVERAGE
A5-4	1.87	3.65–3.75	3.7
A5-6	1.87	3.2–3.4	3.3
A6-4	6.0	3.9–4.0	4.0
A6-5	12.0	5.0–5.2	5.1
A6-9	12.0	5.0–7.0	6.3
A6-6	18.4	8.1–8.5	8.3
A6-7	18.4	7.5–9.0	8.1

TABLE 2.5
VPE LO-HI-LO WAFER DOPING UNIFORMITY

SAMPLE A1-6

PEAK DOPING (cm^{-3})	$Q_s \times 10^{12}$	SPIKE POSITION (μm)	x, y*	V_B
5.2e17	2.85	0.39	8, 9	18 V
4.9e17	2.70	0.39	5, 6	18 V
5.5e17	2.85	0.37	8, 3	16 V
5.0e17	2.76	0.40	3, 9	15 V
AVERAGE 5.15e17 ± 0.26 (± 5.0%)	2.79 ± 0.073 (± 2.6%)	0.39 ± 0.013 (± 3.2%)		

*Row column location on the wafer

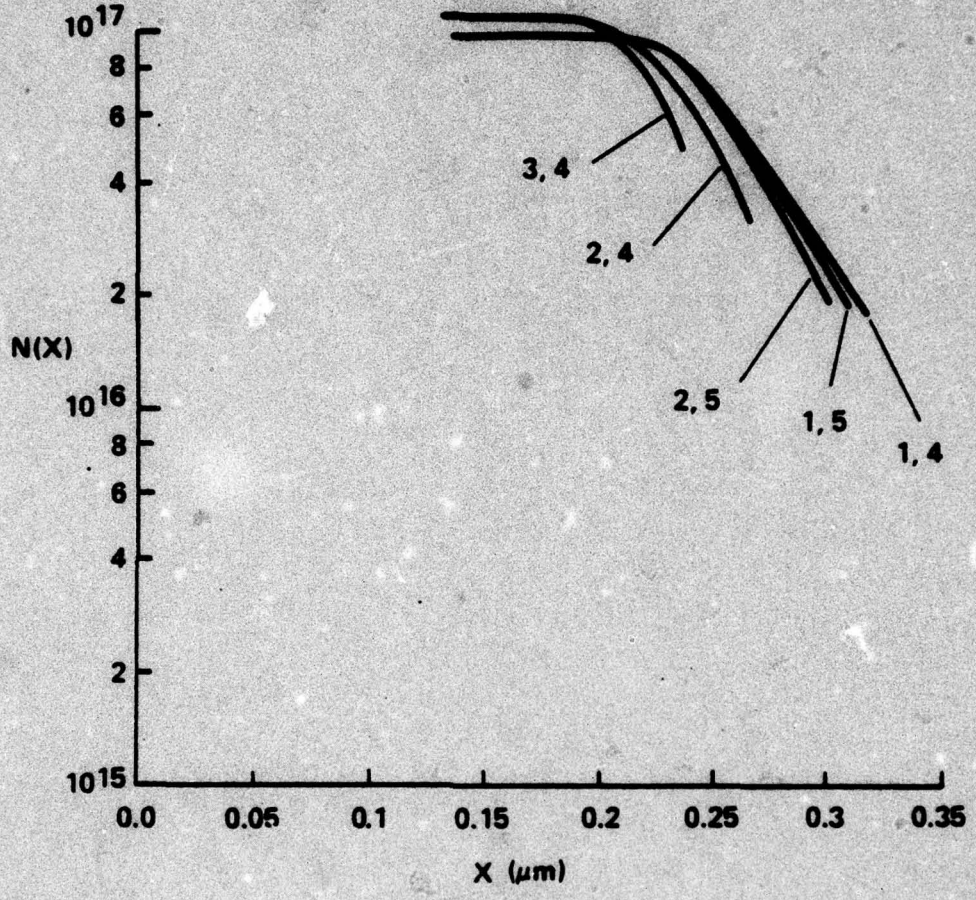


Figure 2.8 Net Effective Profile of VPE p^+ Hi-Lo Wafer

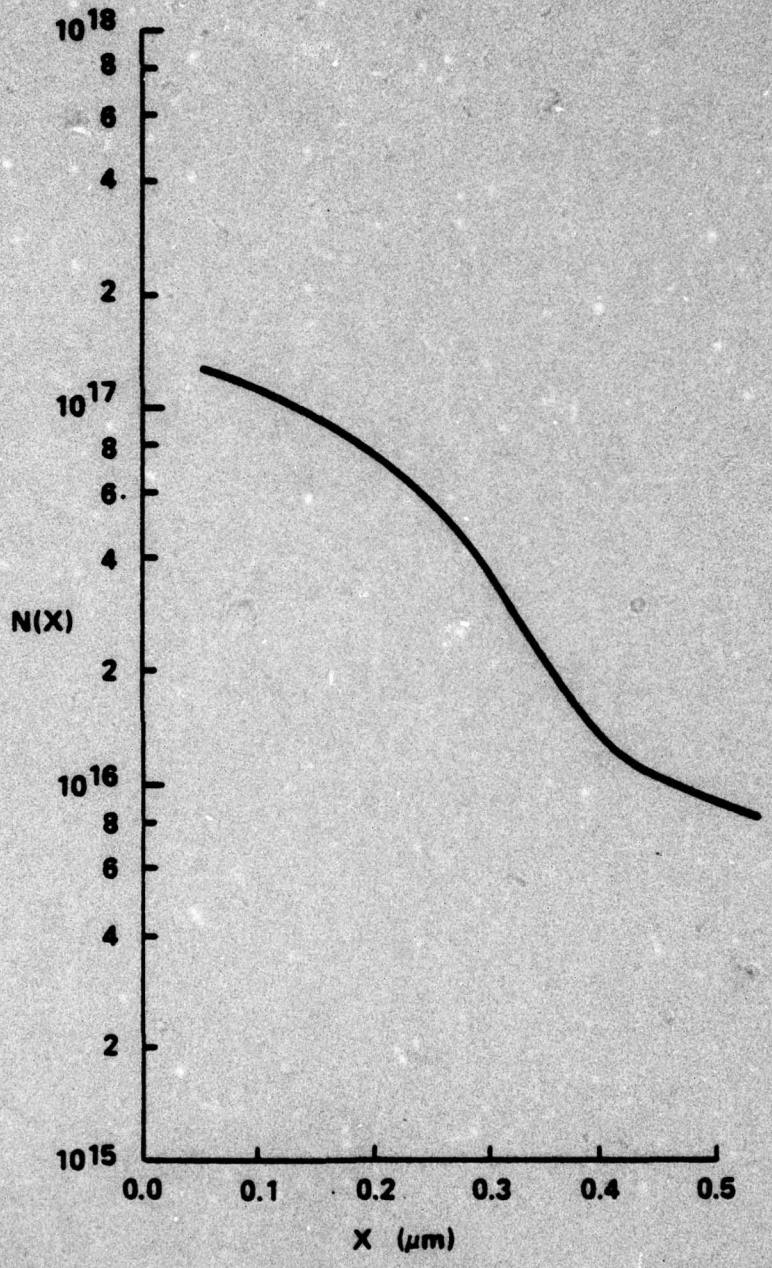


Figure 2.9 N^+ Layer Profile of VPE p^+ Hi-Lo Wafer

3. DEVICE DESIGN, FABRICATION, AND EVALUATION

3.1 STATIC FIELD PROGRAM

A simple static field program using a Hewlett-Packard 9821 desktop calculator was used to establish initial device designs for both the hi-lo and lo-hi-lo doping profiles. The idealized doping and electric field profiles used for these calculations are shown in Figure 3.1.

The breakdown voltages were calculated for an operating temperature of 160°C based on ionization rates determined by Salmer, et al[7]. In both cases, the drift length, $W-X_1$, is calculated for a π transit angle from the following equation:

$$W - X_1 = \frac{V_s}{2f}$$

where V_s is the saturated drift velocity of the electrons at the operating temperature, and f is the frequency. The total epitaxial layer length, W_T, is grown approximately 25% longer than is required for punch-through operation. Increased efficiency is expected by allowing for depletion width modulation in n-type GaAs.

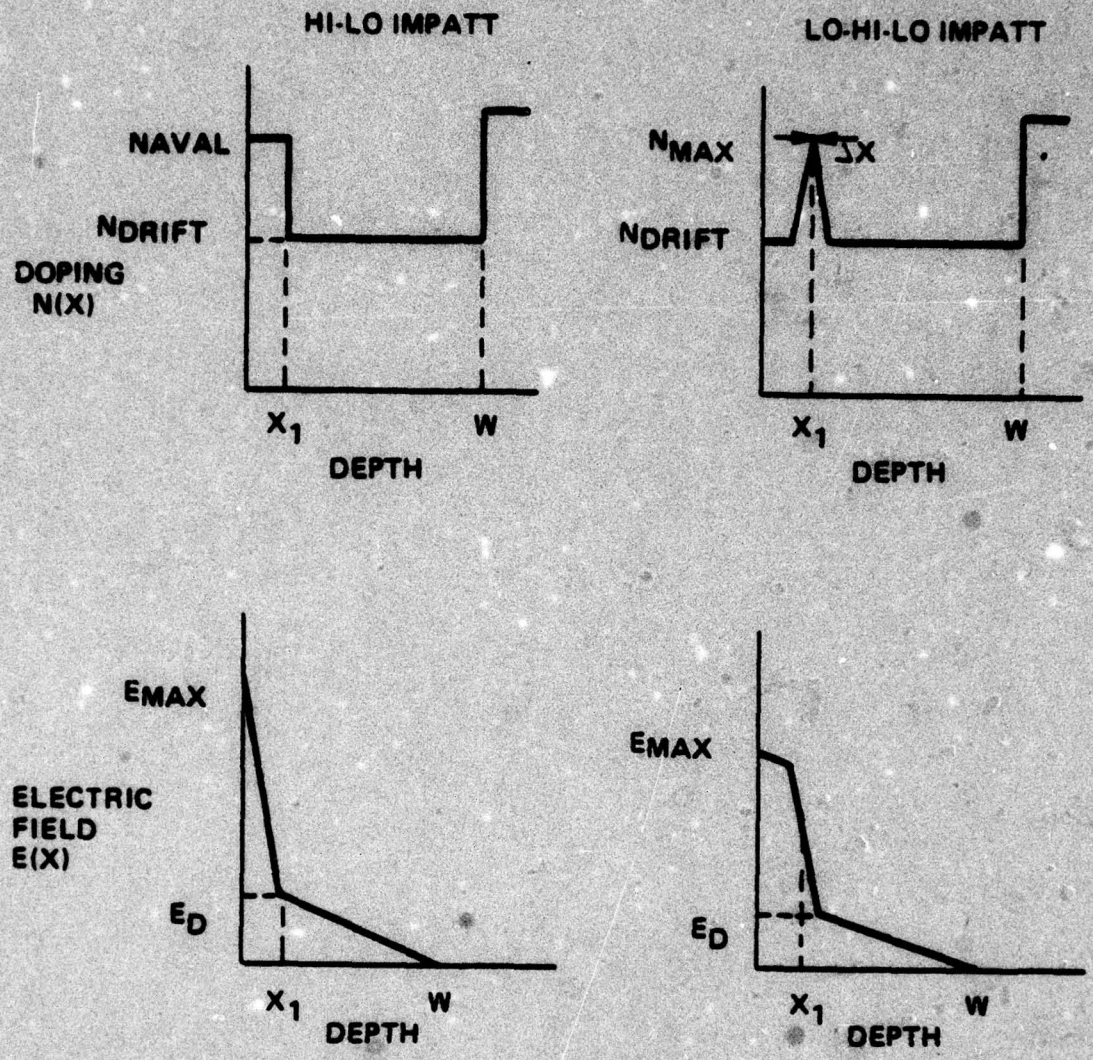
For a given doping profile, the avalanche layer thickness, X_1, can be calculated by performing the following integral,

$$\int_0^{X_1} \alpha(x)dx = 0.95$$

where $\alpha(X)$ is the field dependent ionization rate

$$\alpha(X) = \alpha_\infty e^{-\left(\frac{b}{E(X)}\right)^2}$$

where α and b are temperature-dependent ionization constants.



W = DEPLETION WIDTH

W_T = TOTAL EPITAXIAL LAYER LENGTH

Figure 3.1 Read Profiles

The electric field across the device is calculated from Poisson's equation once the avalanche width has been determined. The corresponding avalanche voltage, V_A, and drift voltage, V_D, can be calculated by integrating the electric field across these zones. A first order estimate of efficiency can be determined from the following equation[8].

$$n = \frac{1}{\pi} \frac{V_D}{V_A + V_D}$$

This equation does not take into account such things as negative differential mobility in GaAs[9], "premature collection"[10] modes, or "surfing" modes[11].

Initial doping designs used for the hi-lo and lo-hi-lo profiles are presented in Tables 3.1 and 3.2 respectively.

Several other factors were considered during the initial device design. First, the electric field at the beginning of the drift zone, E_D, was designed to be in the 150-220 kV/cm range to confine the avalanche zone. Drift layer dopings of $5\text{-}9 \times 10^{15}$ cm^{-3} correspond to these field values at 14 GHz.

Another consideration for the hi-lo design was the electric field directly at the junction, E_{max}. This field is proportional to the avalanche dopings as seen in Table 3.1. A maximum field of 700-725 kV/cm which corresponds to avalanche layer doping of $6\text{-}10 \times 10^{16}$ cm^3 was used to avoid problems of tunneling, excessive leakage currents and poor reliability. The lo-hi-lo design has a significant advantage over the hi-lo design in that narrower avalanche zones can be used without resulting in excessively high electric fields at the junction. As a result, the lo-hi-lo design should be slightly more efficient then the hi-lo design due to its ability to confine further the avalanche process.

Another constraint concerning the optimum avalanche doping for hi-lo structures grown by LPE is the avalanche width X_1. As the avalanche doping is increased, the width decreases due to the higher electric fields. Any small variation in the avalanche zone thickness causes a larger variation in the

TABLE 3.1
INITIAL HI-LO DESIGNS

$N_{AVALANCHE}$ ($\times 10^{16}$ cm^{-3})	X_1 (μm)	E_{max} (kV/cm)	N_{drift} (10^{16} cm^{-3})	EFFICIENCY (%)
6.0	0.603	627	5.0	10.5
8.0	0.494	673	5.0	11.5
10.0	0.425	714	5.0	12.1
6.0	0.544	627	7.0	13.2
8.0	0.449	672	7.0	14.3
10.0	0.389	714	7.0	15.1
6.0	0.485	627	9.0	15.6
8.0	0.404	672	9.0	16.7
10.0	0.353	714	9.0	17.4

T = 160°C
f = 14 GHz

TABLE 3.2
INITIAL LO-HI-LO DESIGNS

$N_{AVALANCHE}$ ($\times 10^{17}$ cm^{-3})	ΔX (Å)	X_1 (μm)	E_{max} (kV/cm)	EFFICIENCY (%)
2.0	200	1.64	430	12.9
2.0	400	1.02	437	14.7
2.0	600	0.59	468	17.4
2.0	800	0.35	506	20.5
4.0	200	0.94	439	14.9
4.0	400	0.31	523	20.5
4.0	600	0.16	652	23.9
4.0	800	0.11	791	25.6
6.0	200	0.50	475	17.8
6.0	250	0.33	514	19.9
6.0	400	0.16	663	23.6
6.0	500	0.12	771	24.7
8.0	100	0.89	441	15.0
8.0	200	0.29	533	20.4
8.0	300	0.15	669	23.4
8.0	400	0.11	815	24.6

$N_{drift} = 7.0 \times 10^{15}$ cm^{-3}
T = 160°C
F = 14 GHz

breakdown voltage and resulting rf performance. During this program, it became evident that the avalanche zone thickness is the most critical parameter in the growth of the hi-lo IMPATT. As the avalanche doping increases, the efficiency increases, but the yield of good diodes decreases due to the larger sensitivity of rf performance to the avalanche zone thickness.

Figure 3.2 is a plot of calculated room temperature breakdown voltage as a function of avalanche width for three avalanche doping levels. A drift doping of 7×10^{15} cm^3 was assumed. Experience has shown diodes with room temperature breakdowns in the range of 25-35 volts work best pulsed at 14 GHz. The voltage sensitivity can be calculated from these curves. As expected, the higher the avalanche doping, the more sensitive the breakdown voltage is to thickness variations.

3.2 DEVICE FABRICATION

Figure 3.3 presents a flowchart of the IMPATT fabrication process. Once the initial designs have been specified with the static field program, the buffer, drift, avalanche and p^+ contact layers are epitaxially grown on (100) oriented substrates. Both LPE and VPE were used for this program. Once the layers are grown, the doping and layer thicknesses are measured using a Miller profiler and the cleave and stain method.

If the wafer is within the specifications, it is prepared for metallization by thinning the substrate to an overall wafer thickness of 45 μm. This is done chemically using a Bromine-Methanol polish. The thinned wafer is then rigorously cleaned in solvents and residual oxides removed. An Au-Ge-Ni metallization is used to contact the n^+ substrate while Ni-Au is used for the p^+ epitaxial layer. Several different metallizations were tried during this program. The results are discussed in the section concerning reliability. The contacts are subsequently alloyed for several seconds in a hydrogen atmosphere.

Test patterns are etched through the metallization to map the wafer for breakdown voltage. The wafer can be rejected at this point if the breakdown voltage falls outside of the range specified. Figure 3.4 presents a wafer map of wafer E557 which was grown for this program.

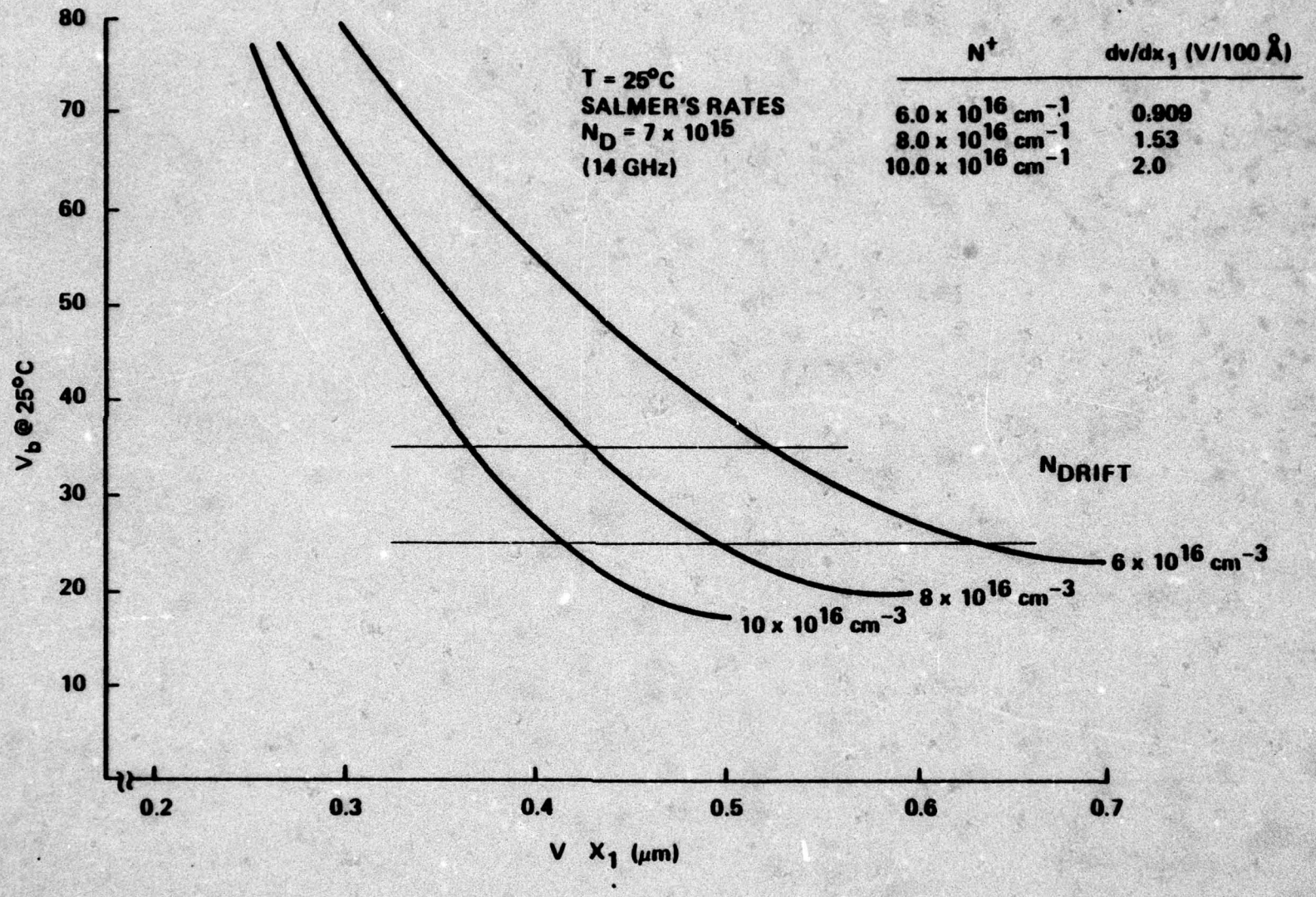


Figure 3.2 Theoretical Breakdown Voltage versus Avalanche Layer Width for Various Drift Dopings

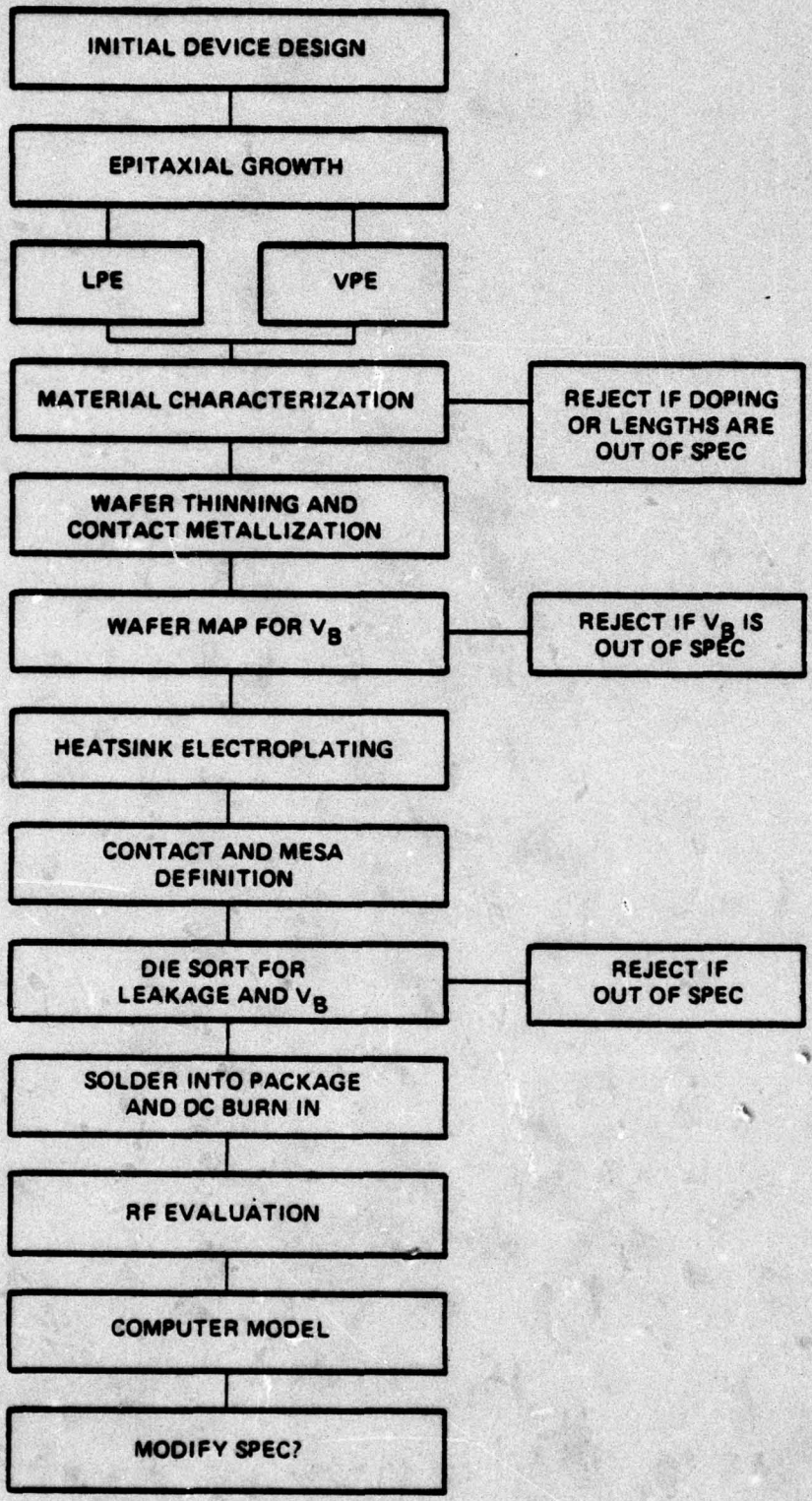


Figure 3.3 IMPATT Process Flow Chart

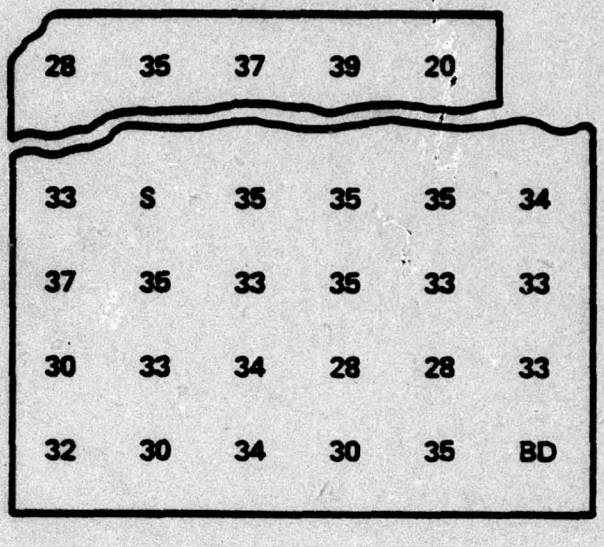


Figure 3.4 Wafer Map of Breakdown Voltage

Once metallized and mapped, the wafer is ready for photolithographic processing. First, integral heatsinks (IHS) are selectively electroplated on the epitaxial side of the wafer. This process, developed at Varian, has the following advantages over traditional IHS processes:

a. No mechanical separation of heat sinks or mesas; thus damage during processing is significantly reduced.
b. Highly controlled heatsink size with virtually no Kerf loss, thus permitting the use of ultra-small or large diode packages as the application requires.
c. Stress-free plating, which eliminates chip strain and microcracks.

The integral heatsink technique utilizes a relatively thick gold pad selectively plated on the active device to obtain uniform thermal contact. The heat generated in the active device enters the metal pad where the thermal flux then spreads to an area sufficiently greater than the active device area to achieve theoretically minimum spreading resistance for the given configuration. Diodes are then etched into mesas using standard photolithographic processes which control the geometry of the mesa. Undercutting or reverse mesa slopes are avoided to minimize the surface fields and prevent premature failure. An SEM photograph of device chips is shown in Figure 3.5. Once etched into separate dies, they are probed for breakdown and leakage. Those dies satisfying the requirements are than soldered onto a gold plated copper stud in the diode package using a gold-tin solder preform in a forming gas ambient. Once the package is sealed, the devices are placed on a dc burn-in to eliminate premature failures.

Finally, the devices are evaluated in a microwave test circuit for power and efficiency. The wafer's doping profile can be entered into a large-signal analysis program for evaluation. On the basis of these results, the initial device design can be modified for improved performance.

3.3 WAFER EVALUATION

Table 3.3 presents a summary of the hi-lo wafers grown by LPE. Initial

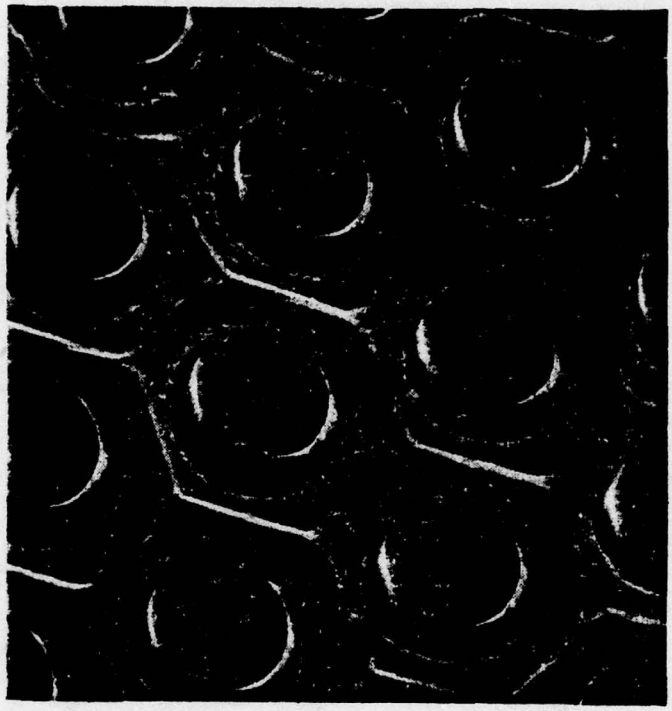


Figure 3.5. SEM Photograph of an IMPATT Wafer after Photolithographic Processing

TABLE 3.3
LPE HI-LO IMPATT WAFERS

WAFER NO./ RUN NO.	n^+ (x 10^{16} cm^{-3})	X_1 (μm)	n^- (x 10^{15} cm^{-3})	V_b	COMMENTS
E421/C600A	5.0	0.42	6.5–8	45–50	High V_b
E422/C601A	4.0	...	6–7	24–38	
E427/C605A	5.5	...	6–8	15–20	Leaky
E434/C612A	5.0	0.5	6–9	18–20	
E440C616A	7.0	...	6	35–60	High V_b
E451/C620A	13.0	0.3	10	13–15	Low V_b
E453/C620A_2*	13.0	0.3	10	15–20	Soft
E469/C626A	7.0	0.3	9	30–40	
E470/C624A_2*	7.0	0.3	9	37–42	
E471/C625A	7.0	...	12	40–45	High V_b
E474/C624A	7.0	0.3	6	48–55	High V_b
E463/C622A	15.0	0.2	13	30–40	Poor dc
E459/C622A_2*	15.0	0.2	13	25–40	Poor dc
E533/C669A	9.0	0.4	4–6	16–20	Low V_b
E539/C670A	8–9	0.3	7–8	15–17	Low V_b
E540/671A	9–10	0.2	7.0	60–75	High V_b
E541/C672A	9.5	0.35	5–6	15–34	
E542/C673A	8–9	0.3	6.5	18–35	Leaky
E548/S567A	8–9	0.35	7.0	...	
E550/C676A	7–9	0.4	7–9	16–25	
E551/C677	7–5	0.4	6–8	30–45	
E552/C678	7–9	0.3–0.35	6–8	40–60	
E553/S569	9	0.2–0.4	5–7	40–78	High V_b
E555/C680A	7–7.5	0.3	6.0	48–78	High V_b
E556/C681A	7–8	0.25	8–9	38–55	High V_b
E557/C682A	7–5	0.3	12.0	28–35	
E558/S571A	7–8	0.3–0.35	6.0	19–45	
E559/C683A	6.0	0.45	6.0	20–35	
E561/C684	8.0	0.25–0.3	7–8	36–50	

*Schottky Barrier

wafers were grown with avalanche dopings near $5\text{-}6\times10^{16}$ cm^{-3}. This was later increased to $7\text{-}8\times10^{16}$ cm^{-3} to confine the avalanche further in order to improve performance. Later profiles were modeled after wafers which had performed well.

Table 3.4 presents a summary of the lo-hi-lo wafers grown by VPE, all of which received Schottky barrier metallizations. Previous attempts to grow a p^+ layer by LPE on VPE lo-hi-lo material failed. The diodes showed poor junction characteristics. Several of the Schottky barrier lo-hi-lo wafers were step-etched in an effort to optimize the diodes' performance experimentally by providing a distribution of spike depths across the wafer. Also, an attempt was made to anodically etch a wafer to specified breakdown voltage before the Schottky barrier was deposited.

Table 3.5 presents a summary of the p^+-hi-lo wafer grown during the last part of the program with VPE. Since the lo-hi-lo profile proved to be very sensitive to spike depth, we felt the hi-lo design was the better way to go in the interest of time. Also, we have had more experience with the hi-lo profile and this would result in a more meaningful comparison of LPE and VPE.

Once each wafer was grown and metallized, the breakdown voltage and doping profile were measured before the wafer was submitted for further processing. Wafers which were outside of a useful range of breakdown voltages or had wrong doping profiles were eliminated at this stage.

Table 3.6 presents a summary of the best rf results obtained from the hi-lo wafers grown by LPE. A total of 26 runs were made with three of the wafers being divided in half for p^+-Schottky comparisons. These results are for the best diodes. They were evaluated at frequencies between 13 and 14 GHz by varying the circuit tuning.

Table 3.7 presents similar data for the lo-hi-lo devices grown by VPE. All devices were Schottky barrier. Upon completion of the modification of the VPE reactor to incorporate cadmium doping, the vapor-phase designs were changed. Instead of trying to grow p^+-lo-hi-lo wafers, the somewhat simpler p^+-hi-lo design was chosen in the interest of time. The results from these VPE wafers are summarized in Table 3.8. Unfortunately, time prevented continuing work with this

TABLE 3.4
VPE LO-HI-LO WAFERS

WAFER NO./ RUN NO.	METALLIZATION	N_{max} ($\times 10^{17}$ cm^{-3})	X_1 (μm)	ΔX (Å)	N_D $\times 10^{15}$ cm^{-3}	V_b (V)
E417/A_2–9$B_{1,2}$	Al-Ti-Pt-Au	5.5	0.2	250	12–13	10–18
E436/A_2–4A_{1-3}	Al-Ti-Pt-Au	3.8	0.31	500	6–8	10–36
E460/A_4–8A_1	Pt-Ti:W-Au	2.4	0.53	500	8–9	20–25
E480/A5–4A_1	Pt-Ti:W-Au	3.8	0.45	350	10	35–38
E487/A_6–4A	Pt-Ti:W-Au	4.0	0.24	475	9.5	44–70
E524/A_6–5AA	Pt-Ti:W-Au	5.0	0.19*	400	7–8	20–30
E525/A_6–6A	Pt-Ti:W-Au	8.0	0.175**	450	7.0	30–50
E526/A_6–7A	Pt-Ti:W-Au	7.5	0.22**	500	7.0	50–70
E544/A_7–8A	Pt-Ti:W-Au	4.5	0.41**	400	10	12–14
E545/A_8–3A	Pt-Ti:W-Au	6.0	0.21**	350	7.0	18–50

*Anodized

**Step Etched

TABLE 3.5
P^+-HI-LO VPE WAFERS

WAFER NO./RUN NO.	n^+ x 10^{16} cm^{-3}	X_1 (μm)	n^- (x 10^{15} cm^{-3})	V_b	COMMENTS
E592/A_{10}4A	9.5–10	0.35	7–8	10–13	V_b too low
E593/A_{10}-5A	11.0	---	10	10–12	V_b too low
E595/A_{10}-6A	10–11	0.25	8–9	17–33	
E596/A_{10}-4B	10	0.35	8	10–14	V_b too low
E597/A_{10}-5B	10	---	8	12–15	V_b too low
E598/A_{10}-6B	13	0.25	7.5	25–45	

TABLE 3.6
RF RESULTS OF LPE HI-LO WAFERS

Pulse Length = 500 nsec
Duty Cycle = 10%

WAFER NO.	PEAK POWER (W)	EFFICIENCY (%)	f (GHz)
E421		High V_b	
E422			
E427	10.0	17.2	13.45
E434	7.3	12.0	14.4
E440		High V_b	
E451*	9.5	23.6	13.65
	19.0	15.2	13.97
	17.0	14.3	14.34
E451	2.8	- - -	14.6
E453**		Low V_b	
E459		Poor dc characteristics	
E463		Poor dc characteristics	
E469	11.75	13.4	13.62
E470**		High V_b	
E471	4.0	9.6	12.6
E474		High V_b	
E533	11.5	24.0	13.3
E539	13.75	18.6	13.9
E540		Notch after hi region	
E541	7.8	23.1	13.3
E542		Leaky breakdown	
E550	7.0	21.9	14.5
E551	17.0	22.4	13.1
$E551X_1$	17.5	20.0	13.0
	16.5	21.0	13.62
$E551X_2$	14.0	20.3	13.45
E552		High V_b	
E553		High V_b	
E555		High V_b	
E556		High V_b	
E557	12.25	14.1	13.55
E558		High leakage	
E559	20.5	21.1	13.1
	16.0	19.1	13.9
E561	11.0	14.7	13.7

*Wafer grown for Air Force program
**Schottky barrier

TABLE 3.7
RF RESULTS OF VPE LO-HI-LO WAFERS

Pulse Length = 500 nsec
Duty Cycle = 10%

WAFER NO.	PEAK POWER (W)	EFFICIENCY (%)	FREQUENCY (GHz)
E417		Low V_b	
E436	8.75	9.0	11.6
E460	4.0	5.8	12.3
E480		High V_b	
E487		High V_b	
E524	4.0	10.7	12.0
E525	7.6	12.2	13.9
	4.5	14.3	15.2
E526		High V_b	
E544		Low V_b	
E545	15.0	14.2	13.86

TABLE 3.8
RF RESULTS OF VPE p+ HI-LO WAFERS

WAFER NO.	PEAK POWER (W)	EFFICIENCY (%)	FREQUENCY (GHz)
E592		Low V_b	
E593		Low V_b	
E595	1.8	10.2	14.05
E596		Low V_b	
E597		Low V_b	
E598	7.8	8.1	14.3

design at 14 GHz. It was felt that the more uniform VPE material as well as the ability of the microprocessor-controlled reactor would result in considerable improvements in overall diode yield. Work in this area has continued with company-funded money for designs centered at 9 GHz. Efficiency of 29% with power of 17.8 W at 9.5 GHz was the best result measured to date. This is in agreement with the similar p^+-hi-lo design grown by liquid phase.

Once each wafer was evaluated for rf performance, the doping profiles were examined to find why one wafer worked better than another. Packaged devices were measured for capacitance as a function of voltage. The packages were opened and the junction areas were measured optically to calculate the doping profiles from the C-V measurements. A more rigorous computer analysis program was used to correlate theoretical performance with experimental.

Instead of using an idealized doping profile as in the static field design program described earlier in the report, the actual doping profile could be entered point by point. Also included in this analysis were the effects caused by space charge resistance and current density. The program calculated electric field distribution and breakdown voltages [12] on the basis of the doping profile and the ionization rates determined by Salmer. Also, by solving the equations determined by Misawa[13], small signal impedances could be calculated for the device.

Figure 3.6 presents an example of doping profiles for two of the better performing hi-lo wafers. These doping profiles were entered into the computer program point by point with the result for E551 shown in Figure 3.7. The current density was assumed to be 1000 A/cm^2 while the saturation current density is 1 A/cm^2. Ionization rates determined by Salmer are also used.

Table 3.9 presents a summary of the predicted results versus those observed experimentally. There appears to be good agreement for breakdown and operating voltage indicating that the electron ionization rates determined by Salmer are reasonably accurate.

The analysis program was also used for the lo-hi-lo IMPATT design where it was very useful in determing the spike position. The ability to enter the profile point by point proved to be more accurate than the idealized profile used

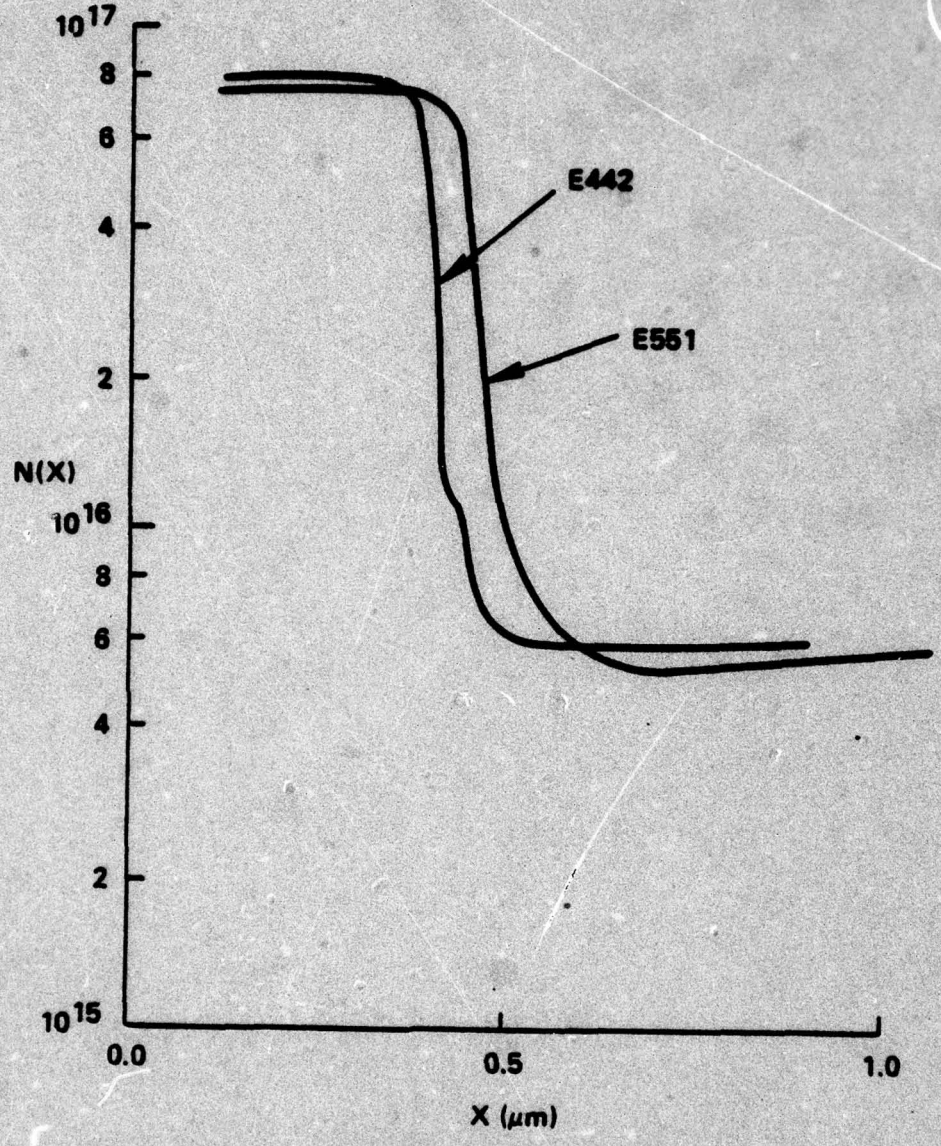


Figure 3.6 Doping Profiles of Two P^+ Hi-Lo Wafers

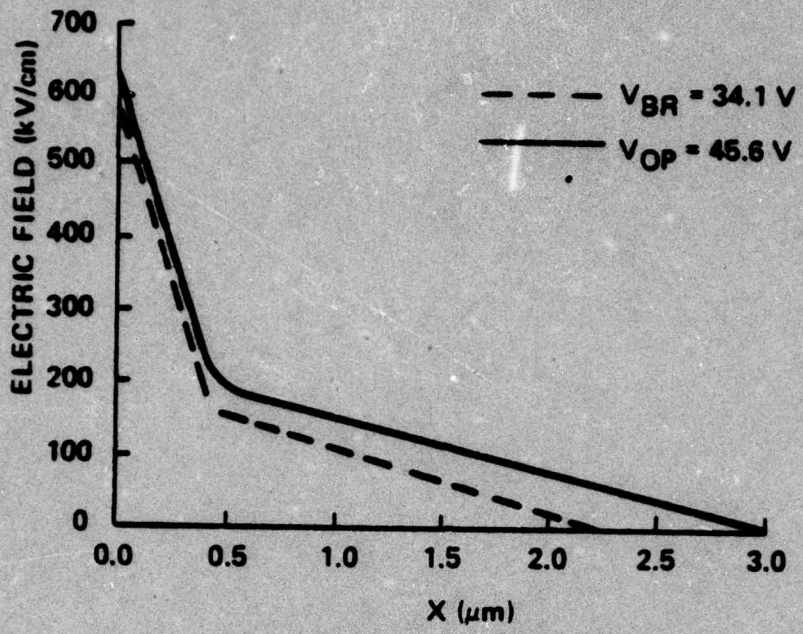


Figure 3.7A Electric Field of E551

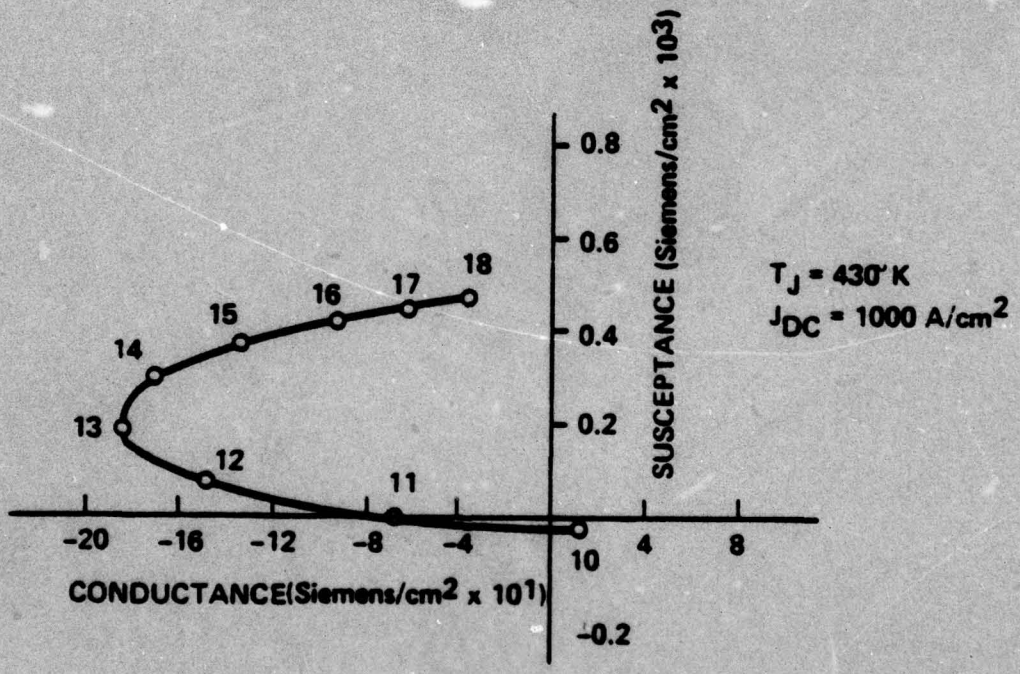


Figure 3.7B Theoretical Small Signal Admittance of E551

TABLE 3.9
THEORETICAL VERSUS EXPERIMENTAL RESULTS

WAFER	V_{br} @ 25°C		V_{op} @ 160°C		$f_{(opt.)}$ GHz	
	THEORY	EXPERIMENTAL	THEORY	EXPERIMENTAL	THEORY	EXPERIMENTAL
E442	37.9	32.0	46.9	44–45	14	13.9–14.2
E551	34.1	32.0	45.6	42–44	13	13–14

for the static field optimization program. The one limitation was that the depletion width resulting from the built-in potential of the junction prevented the front of the spike from being profiled. As a result, it was assumed to be symmetric.

Since time did not allow full characterization of the VPE reactor for the p^+ material growth, all the lo-hi-lo material received a Schottky barrier of one type or another. This had the advantage of allowing the wafer to be chemically etched before the barrier was deposited to optimize the spike position. The wafer could be grown with the spike intentionally placed too deep, and then profiled. The analysis program could predict the spike position for optimum performance.

Table 3.10 presents the results from the program for a typical lo-hi-lo wafer. The negative conductance and chip Q are presented for three frequencies as the spike is moved closer to the surface. It appears that the optimum spike position is 0.175 μm from the junction. Any closer to the surface results in "spill-over" and the avalanche process is no longer confined to this zone. The small signal impedance of the chip has a minimum Q at this value indicating optimum rf performance.

The analysis program proved to be very useful in determining why some wafers worked better than others. While the original static field program provided an optimum design for given doping levels, the analysis program included more parameters and predicted results close to those observed experimentally.

Figure 3.8 shows the peak power and efficiency for one of the better hi-lo wafers as function of duty cycle. The pulse length was 1 microsecond. It appears that E442 has a maximum efficiency when the junction temperature corresponds to a duty cycle of about 15%. The effect of the higher duty cycles and temperatures is seen in the drop of optimum operating frequency. Most wafers exhibited similar performances as a function of duty cycle and junction temperature. There seem to be two factors which affect the rf performance. First, as the duty cycle is decreased from 25% to 10%, the power increases and the efficiency remains fairly constant. At the lower operating temperatures, the device is able to operate at higher current densities while still remaining in the high

TABLE 3.10
STATIC FIELD PROFILE DESIGN FOR WAFER A5-4A

$T = 430°K$ $J_{DC} = 1000\ A/cm^2$ $J_s = 1\ A/cm^2$

$V_e = 6 \times 10^6$ cm/sec $V_h = 7 \times 10^6$ cm/sec (Equal rates of Salmer, et al)

X_p (μm)	X_A (μm)	W_T (μm)	E_m 9 (kV/cm)	G(13)/Q(13)	G(14)/Q(14)	G(15)/Q(15)	V_A	V_T	η S-G
0.295	0.266	1.81	519.2	−127.9 / −2.29	−143.3 / −2.14	−149.7 / −2.14	14.9	33.8	17.8
0.255	0.232	1.93	533.6	−136.4 / −1.99	−153.4 / −1.99	−158.8 / −1.99	13.8	35.8	19.6
0.215	0.200	2.07	551.8	−147.3 / −3.04	−165.8 / −1.87	−168.5 / −1.88	12.6	38.8	21.5
0.175	0.171	2.25	574.1	−161.3 / −2.00	−180.2 / −1.82	−176.1 / −1.86	11.2	42.8	23.5
0.135	0.166	2.45	599.8	−180.8 / −1.96	−188.4 / −1.84	−168.1 / −1.99	10.9	48.4	24.7
0.115	0.225	2.56	610.7	−173.2 / −1.96	−169.9 / −1.94	−143.9 / −2.19	12.8	51.6	23.9

X_P = Depth of Spike from Junction
X_A = Avalanche Width
W_T = Total Depletion Width
Em = Maximum Electric Field
G(f) = Conductance

V_A = Avalanche Voltage
V_D = Drift Voltage
$\eta_{S\text{-}G}$ = Efficiency

$$= \frac{1}{\pi} \frac{V_D}{(V_A + V_D)}$$

J_{DC} = DC Current Density
J_s = Saturation Current Density
V_e = Saturated Electron Density
V_h = Saturated Hole Velocity

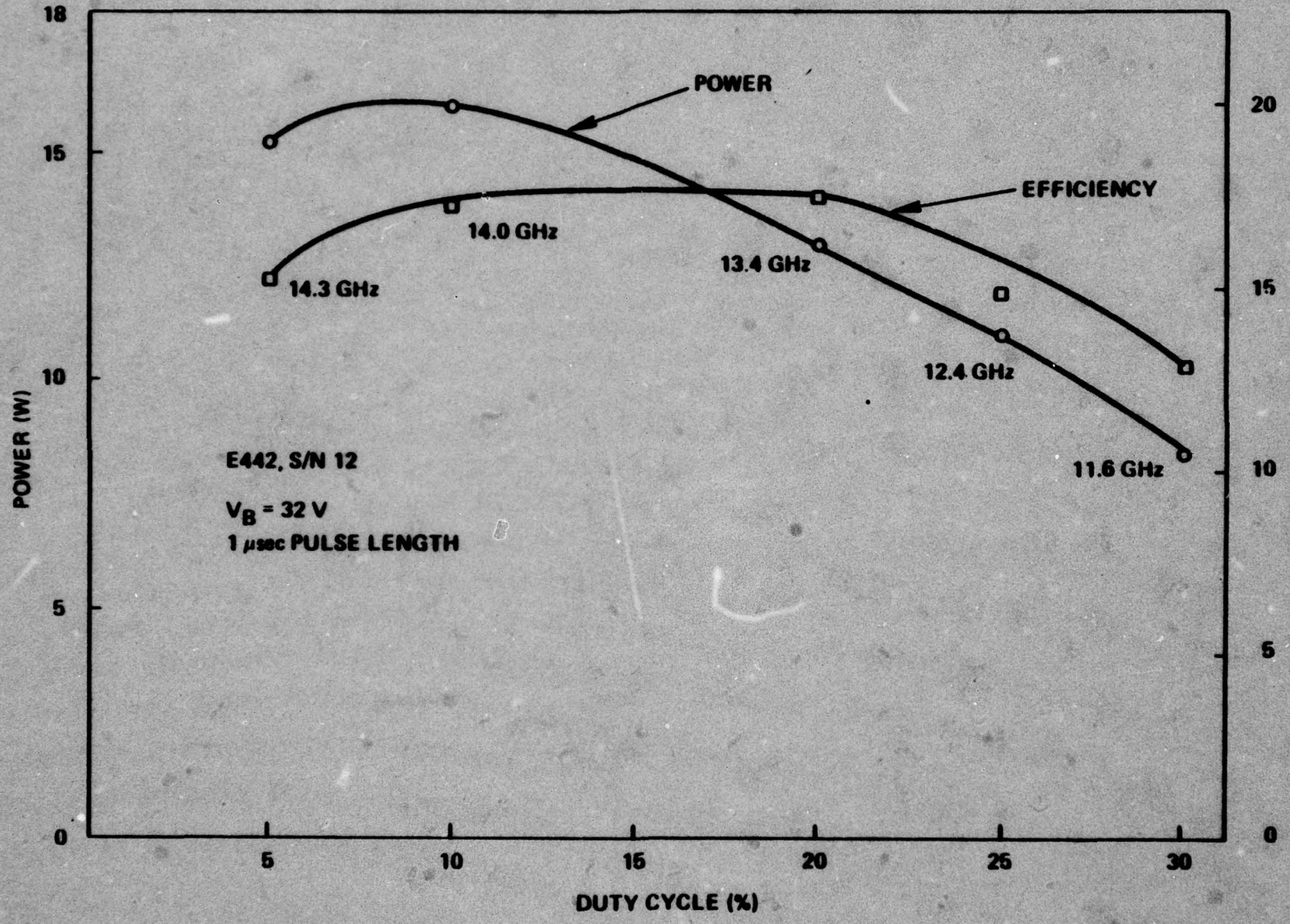


Figure 3.8 Peak Power and Efficiency as a Function of Duty Cycle for Wafer E442

efficiency mode. More power can be put into the device while keeping the same junction area and circuit matching constraints. Thus, the output power increases until a point when the operating voltage is low enough that the efficiency drops. At duty cycles less than 10%, the efficiency is dropping due to a non-optimum electric field profile.

In summary, the LPE hi-lo wafers gave better performance than the VPE lo-hi-lo wafers. We feel this is due mainly to greater experience with the hi-lo profile with LPE. While the lo-hi-lo design should have several advantages, optimum performance was not obtained. More experience with the vapor-phase approach to this design should yield comparable, if not better, results. On the other hand, the lo-hi-lo design is more sensitive to layer thickness than the hi-lo design which adversely affects the overall yield. The breakdown voltage varies from 4 to 5 volts per 100 angstrom variation in spike depth compared to 1 or 2 volts per 100 angstrom for the hi-lo design.

3.4 SCHOTTKY BARRIER RELIABILITY

During the course of this program, a number of different Schottky barrier metallization schemes were investigated in an attempt to find one with acceptable metallurgical stability. It is well known that platinum reacts with GaAs at relatively low temperatures to form a variety of Pt-Ga and Pt-As compounds[15]. As a result of this metallurgical reaction, thermal aging of the Pt Schottky barriers is a problem. The mean-time-to-failure for Pt Schottky barriers is reported to be 4000 hours at 250^{o}C in comparison to 10^5 hours for grown junction IMPATTs[16]. Schottky barriers, on the other hand, do have the advantage of somewhat lower thermal resistance. Also, the highest dc-to-rf conversion efficiencies reported to date have been obtained with Pt Schottky barriers. Thus, it is clear that development of a reliable Schottky barrier metallization for GaAs IMPATTs is warranted, in spite of the reliability advantage of the grown junction.

Several possible metallization schemes for GaAs IMPATTs have been suggested in the literature. One suggested scheme is to employ a thin platinum Schottky barrier in conjunction with a tungsten (W) layer to limit the Pt-GaAs reaction [17]. The other possibility is to employ a more stable Schottky barrier

metal, such as aluminum (Aℓ)[18]. We have evaluated both of these possibilities.

Three metallization systems have been evaluated: GaAs: Aℓ-Ti-Pt-Au, GaAs: Pt-Ti-Au, and GaAs: Pt-TiW-Au. These metallization systems were evaluated on GaAs wafers having a lo-hi-lo doping profile, as it was convenient to employ the position of the donor spike within the material as a "built-in" reference against which to gauge the movement of the electrical junction[19].

In order to prevent gold from diffusing into the junctions at elevated temperatures, diffusion "barrier" metals were placed between the Schottky barrier contact and outer layer of gold. Since the compound Ti_3Pt is known to be an excellent diffusion barrier to gold[20], Ti-Pt was employed as a barrier metal on both Aℓ and Pt Schottky barriers. Since tungsten is also a good diffusion barrier to gold[21], a 1200 Å Ti (10%):W barrier was also employed for the Pt Schottky barriers. A Ti:W alloy was selected because of its improved adherence in comparison to pure tungsten.

Initially the thickness of the Aℓ and Pt Schottky barrrier metallization was 1200 Å. However, passive life tests performed on wafers E435, E436 and E437 indicated that a severe "chew-in" of the junction was occuring at 205°C after 24 hours. Increasing the temperature to 275°C resulted in failure of al Al-Ti-Pt-Au and Pt-Ti-Au junctions within five hours by shorting or excessive leakage. An additional two hours at 300°C caused the junctions with Pt-TiW-Au to become excessively leaky, but resulted in no catastrophic failures. Therefore, it was decided to adopt the Pt-TiW-Au metallization for the remaining wafer metallizations, but to reduce the Pt thickness to 500 Å.

Passive life tests were performed on wafers E460 and E461 which had 500 Å Pt Schottky barriers. These life tests were conducted at an ambient temperature 300°C. Breakdown voltage, saturation current, and doping profile were monitored for a period of 40 hours. No catastrophic failures were recorded in this time period; however, the saturation current had increased to 1 mA. The process of junction chew-in is documented in Figure 3.9a. The data shows that after approximately 10 hours, the initial rapid chew-in of the Pt ceased and a much slower secondary reaction proceeded through 40 hours. This result suggested that that the Ti:W was also reacting with the GaAs. In order to test this hypothesis,

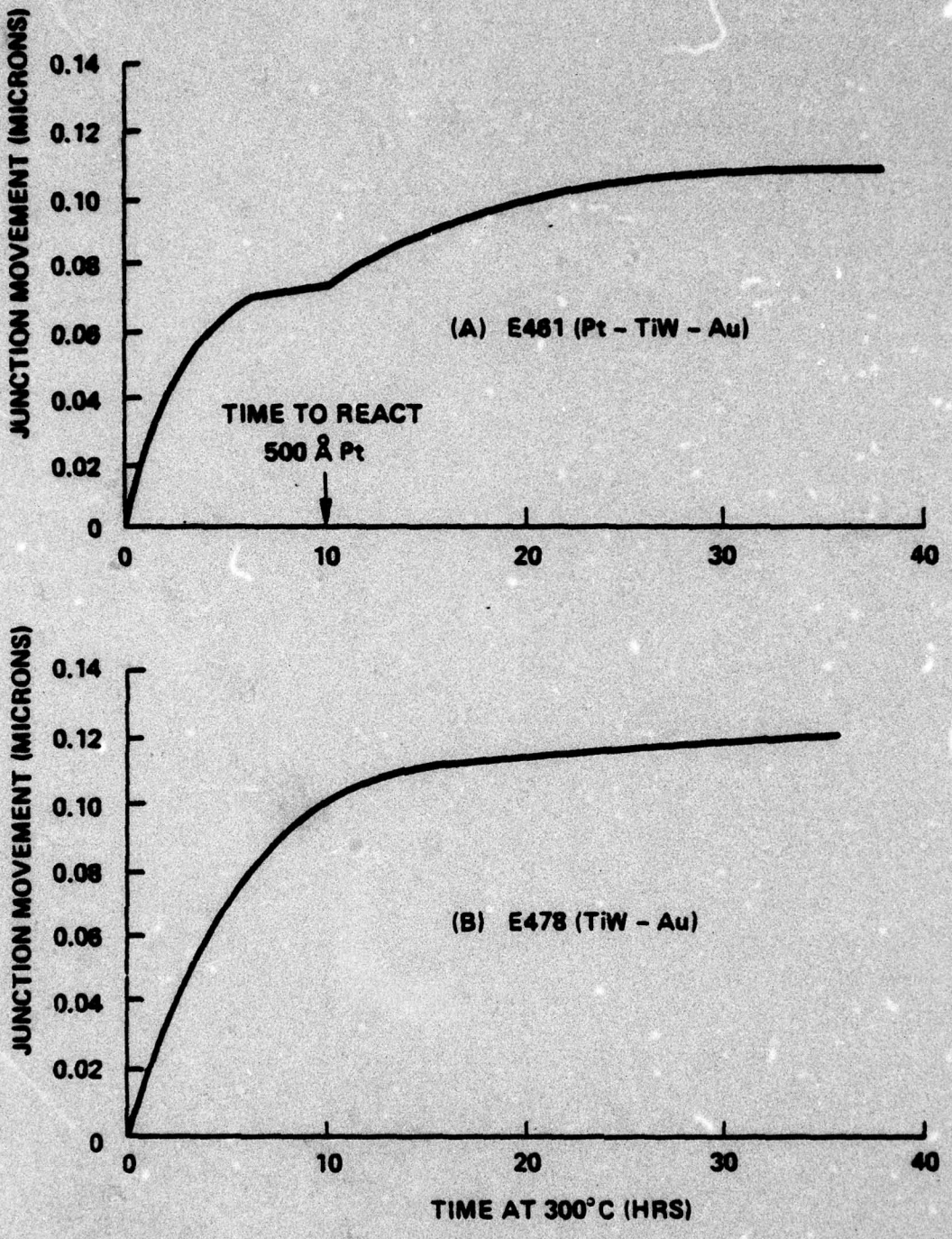


Figure 3.9 Schottky Barrier Junction Movement as a Function of Time at 300°C

wafer E478 was directly metallized with 1200 Å of Ti:W to form the Schottky barrier. Chew-in of the Ti:W metallization is documented in Figure 3.9b. Apparently, reaction of the Ti with the GaAs is responsible for the chew-in, since W/n-GaAs contacts have been reported to be metallurgically stable up to 500°C[21]. Because a pure tungsten target was not available for our sputtering system at the time of this program, we were unable to test this hypothesis further.

The results of our Schottky barrier life test studies may be summarized as follows: Al-Ti-Pt-Au does not appear to be a reliable metallization scheme for high-power Schottky barrier IMPATTs due to a metallurgical reaction with the GaAs. Although the exact nature of the reaction has not been characterized in this study, several possible reactions have been reported in the literature[22,23]. Pt-Ti-Au is not as reliable a metallization as Pt-TiW-Au, probably due to a reaction of the Ga, which dissolves in the Pt, with the titanium[24]. Pt-TiW-Au was the most reliable contact investigated. Its reliability appears to be limited by the presence of Ti in the tungsten alloy. Further investigation is warranted in this area based on these experimental results.

3.5 SCHOTTKY BARRIER AND P^+ GROWN JUNCTION COMPARISON

A number of the LPE hi-lo IMPATT wafers were divided into two sections for a comparison of a Schottky barrier with a p^+ grown junction. A parallel comparison with the same wafer should have given results unbiased by material variations. Evaluation of the Schottky barrier and p^+ grown junctions consisted of measurement of the dc breakdown characteristics, in particular, the reverse saturation current. Thermal resistances were measured. Passive life tests were performed in order to estimate a mean-time-to-failure at elevated ambient temperatures for the two device types. RF performance was evaluated and the "turn-on" characteristics of the rf pulse were examined for delays associated with Schottky barriers[25].

Two problems were encountered which affected a fair comparison of the Schottky barrier and p^+ grown junctions. One problem was the Schottky barrier versions of the first few wafers exhibited poor dc characteristics due to poor Schottky barriers. Modifications to the sputtering system and to the metalli-

zation system employed as a Schottky barrier greatly improved the quality of the junctions on later wafers. Leakage currents as low as 1 nanoampere were observed with diodes from several of these wafers. Secondly, an "etch-back" of the avalanche zone when growing the p^+ layer with LPE was experienced. Figure 3.10 shows the doping profile calculated from C-V measurements of a Schottky barrier (E446) and p^+ grown junction (E438) from the same wafer. The avalanche layer thickness of the Schottky version is almost 0.1 μm longer than the p^+ version, resulting in a much lower breakdown voltage (27 volts for the Schottky versus 50 volts for the p^+ version). The "etch-back" of the avalanche zone sufficiently modified the doping profiles so that only a comparison of dc characteristics was meaningful in most cases.

Figure 3.11 presents typical reverse breakdown characteristics for Schottky barrier and p^+ grown junctions on the same LPE wafer C626. The Schottky barrier contact is Pt-TiW-Au in this case. The photographs clearly show the "soft" breakdown characteristics of the Schottky barrier in comparision to the abrupt breakdown characteristic of the p^+ grown junction. Reverse saturation current of the p^+ grown junction is in the nanoampere range up to one volt of breakdown, while the reverse current of the Schottky barrier is in the microampere range. Aside from observation of a higher incidence of tuning-induced failures with Schottky barriers, it was not possible to correlate microwave performance with reverse saturation current due to the etch-back problem.

Thermal resistance was measured for the Schottky barrier and p^+ grown junctions. On an equal area basis, the Schottky barrier junctions had a thermal resistance $0.75^{o}C/W$ smaller than the p^+ junctions for a junction area of 7×10^{-4} cm^2 and a one micron p^+ contact thickness.

Accelerated passive life tests were performed on Pt Schottky barrier and p^+ grown junctions. Our life-test results with Pt Schottky barriers are in agreement with previously reported data[16].

The degradation of p^+ grown junctions is believed to be related to the simultaneous indiffusion of gold from the Ni-Au p^+ contact and gallium outdiffusion from the GaAs. In order to test this hypothesis, the Ni-Au p^+ contact was replaced with a Pt-TiW-Au Schottky barrier contact on several p^+ grown junction

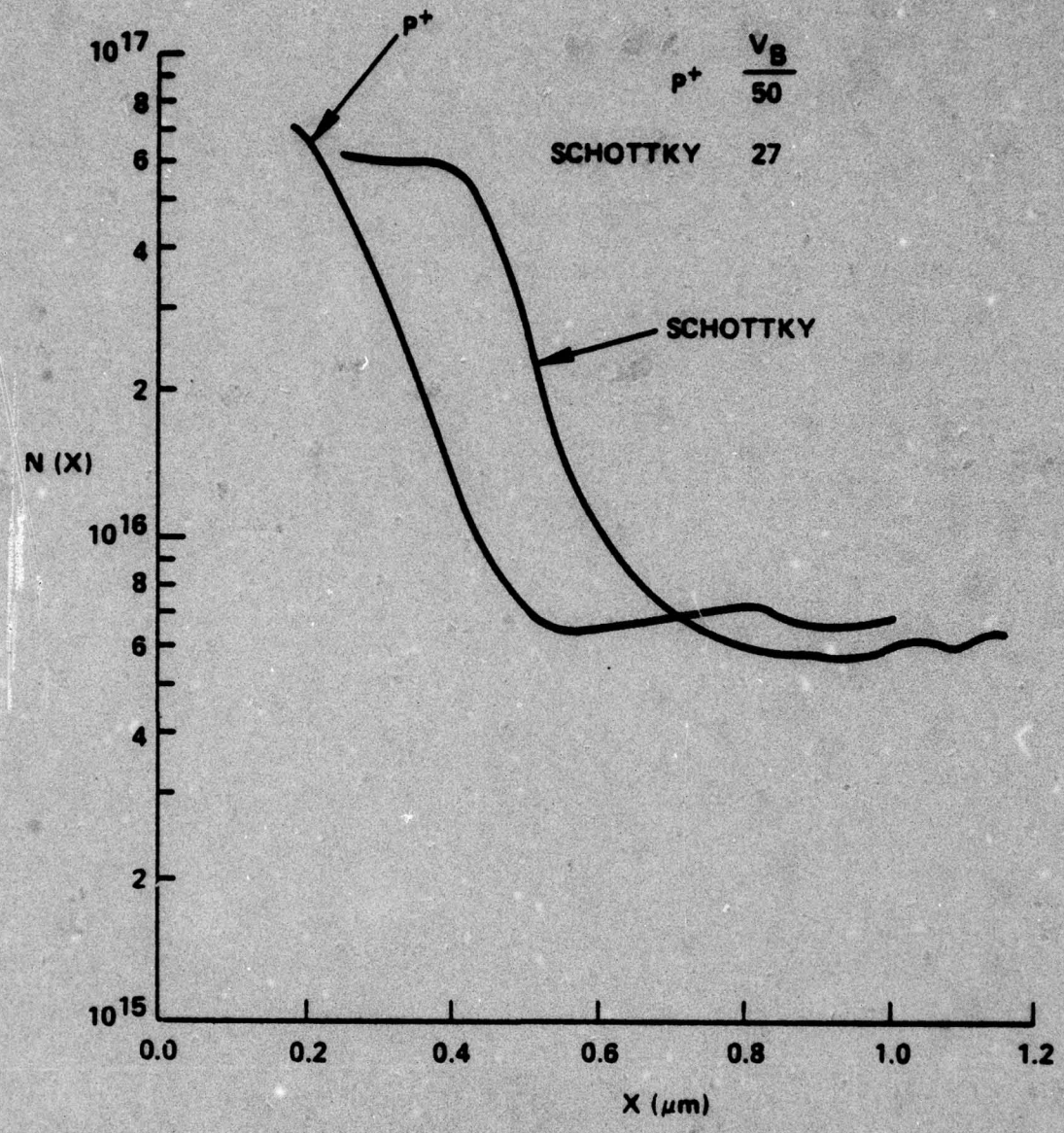
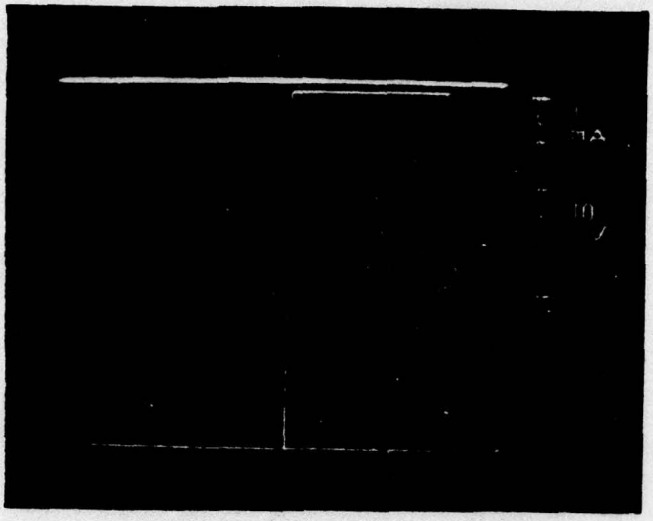
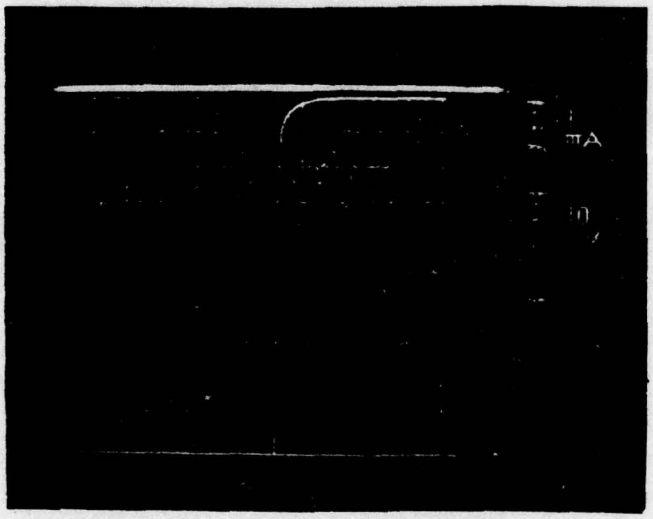


Figure 3.10 P^+ and Schottky Barrier Profiles of Diodes From The Same LPE Wafer



(a) E472 (p^+ Grown Junction on C626)



(b) E473 (Pt Schottky Barrier on C626)

Figure 3.11. Reverse Breakdown Characteristics of p^+ Grown Junction and Pt Schottky Barrier Junction on the Same Wafer

devices. These devices were passively aged at 350° and 375°C. The results of these life tests are shown in Figure 3.12. The failure criterion for the Ni-Au contacted p^+ grown junction devices for 15 mA of reverse leakge current, while the failure criterion for the Pt-TiW-Au contacted devices was only 1 mA. Clearly, a significant improvement in reliability was obtained with the Pt-TiW-Au contact. At 250°C the median time to failure was increased from 10^5 hours to $5x10^5$ hours.

Figure 3.13 is an example of rf pulses from a Schottky barrier diode and a p^+ junction diode. There is no evidence of delayed "turn-on" characteristics observed with the Schottky barrier diode. Rise times are on the order of the current pulse rise time (30 nsec) and equal to the p^+ junction's rise times.

BURN-IN PROCEDURES

While only a limited amount of effort was directed toward evaluating the usefulness of burn-in procedures, some conclusions can be drawn from the observations made. Two types of burn-in were employed during this effort. A passive burn-in was conducted by baking devices in a hydrogen ambient at 300°C for 48 hours. Active burn-in was also evaluated. This consisted of biasing devices under rf stable load conditions with approximately 10 W of dc power. Heat sink temperatures were typically 50-60°C under this condition. Burn-ins were generally carried out for a 48-hour period.

A strong correlation between junction quality and lifetime under the passive stress was observed. Devices that exhibited leakage caused by junction defects (see Section 2) would significantly increase in leakage during the 48-hour bake and would, in some cases, short. Devices with low leakage grown by a process which did not produce junction defects would always survive the 48-hour bake with no degradation and would generally be capable of lasting 10^3 hours at this temperature.

Results from the dc burn-in were not as conclusive. While leaky devices would occasionally fail under this stress, some devices that would clearly fail the passive test would pass the dc burn-in. Apparently, higher heat sink temperatures are required to stress these devices adequately.

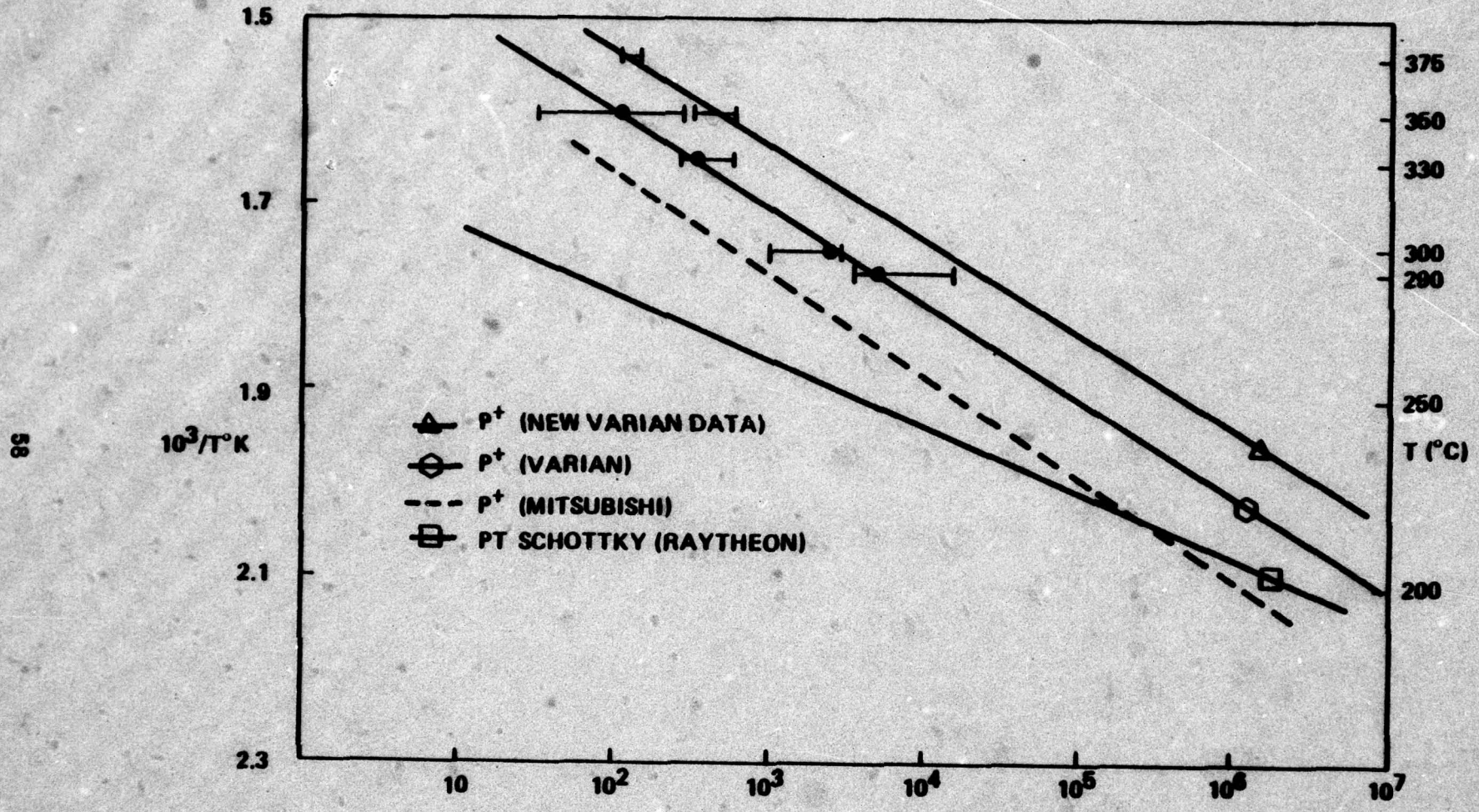
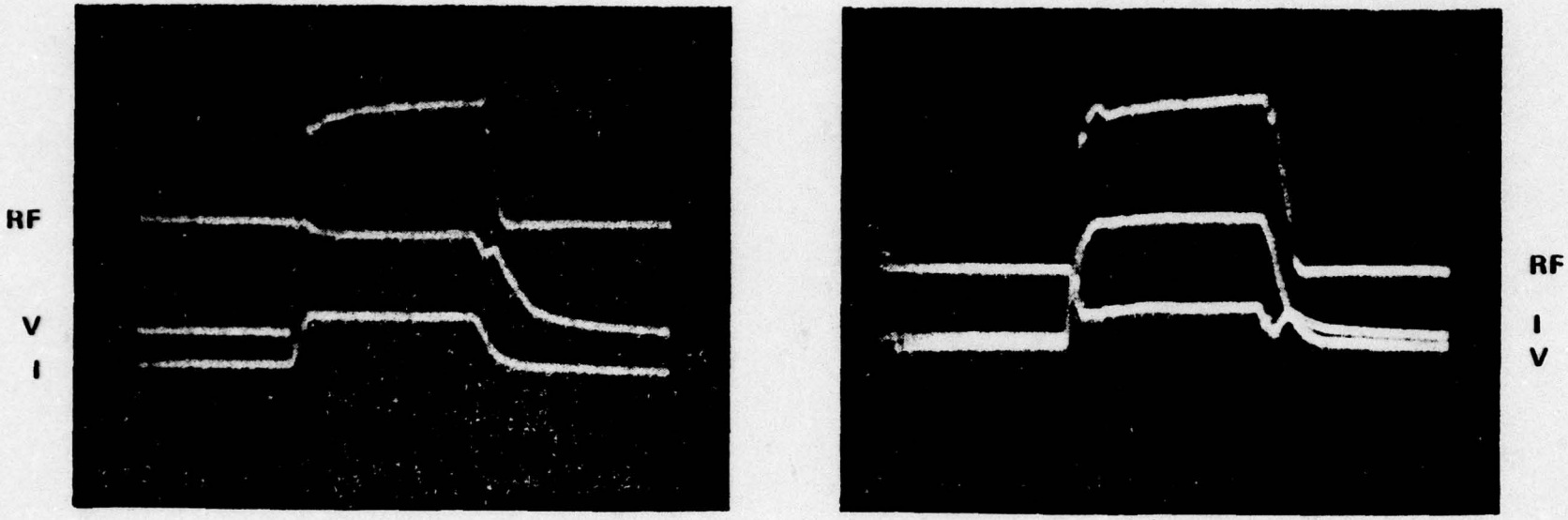


Figure 3.12 Median Time to Failure



SCHOTTKY BARRIER HI-LO
HORIZ = 200 nsec/DIV

P^+ GROWN JUNCTION HI-LO
HORIZ = 200 nsec/DIV

Figure 3.13. Current, Voltage and RF Pulses of IMPATT Diodes

4. CIRCUIT AND PACKAGE DEVELOPMENT

4.1 CIRCUIT DESIGN

A circuit consisting of a coaxial line coupled to a waveguide, pictured in Figure 4.1, was used to evaluate the devices. It is similar to one proposed by Kenyon[26] and Kurokawa[27]. As seen in Figure 4.2, the diode is placed at the end of a section of coaxial line which is terminated in a low pass filter used for biasing. Originally, a microwave absorber was used, but the filter arrangement proved to be less lossy while still eliminating bias instabilities. Irises of various diameters were tried to vary the cavity coupling to the waveguide, but it was found that no iris gave good results for this reduced-height cavity. A non-contacting sliding short and a slide screw tuner were used to optimize performance.

Since this one circuit was used to evaluate wafers with a range of parameters, it was designed to be as flexible as possible to match each wafer optimally. The diameter and length of the coaxial line section could be varied to change the real and reactive parts of the circuit match. Also, the position of the diode with respect to the bottom of the waveguide could be varied by changing the sleeve length. The variation had the largest effect on the circuit reactance.

Overall, this circuit gave repeatable results and was able to match the low values of impedance associated with the larger area pulsed devices. A coaxial circuit was evaluated at 14 GHz for an earlier program with the Air Force. Performance at 14 GHz was difficult to obtain with a single transformer in a 50-ohm system due to the high reactance of the single-drift diodes.

When diodes with pre-breakdown capacitances of 3 picofarads are used, the transformer must be on the order of 1/8 of a wavelength. A transformer shorter than this yields only marginally better results.

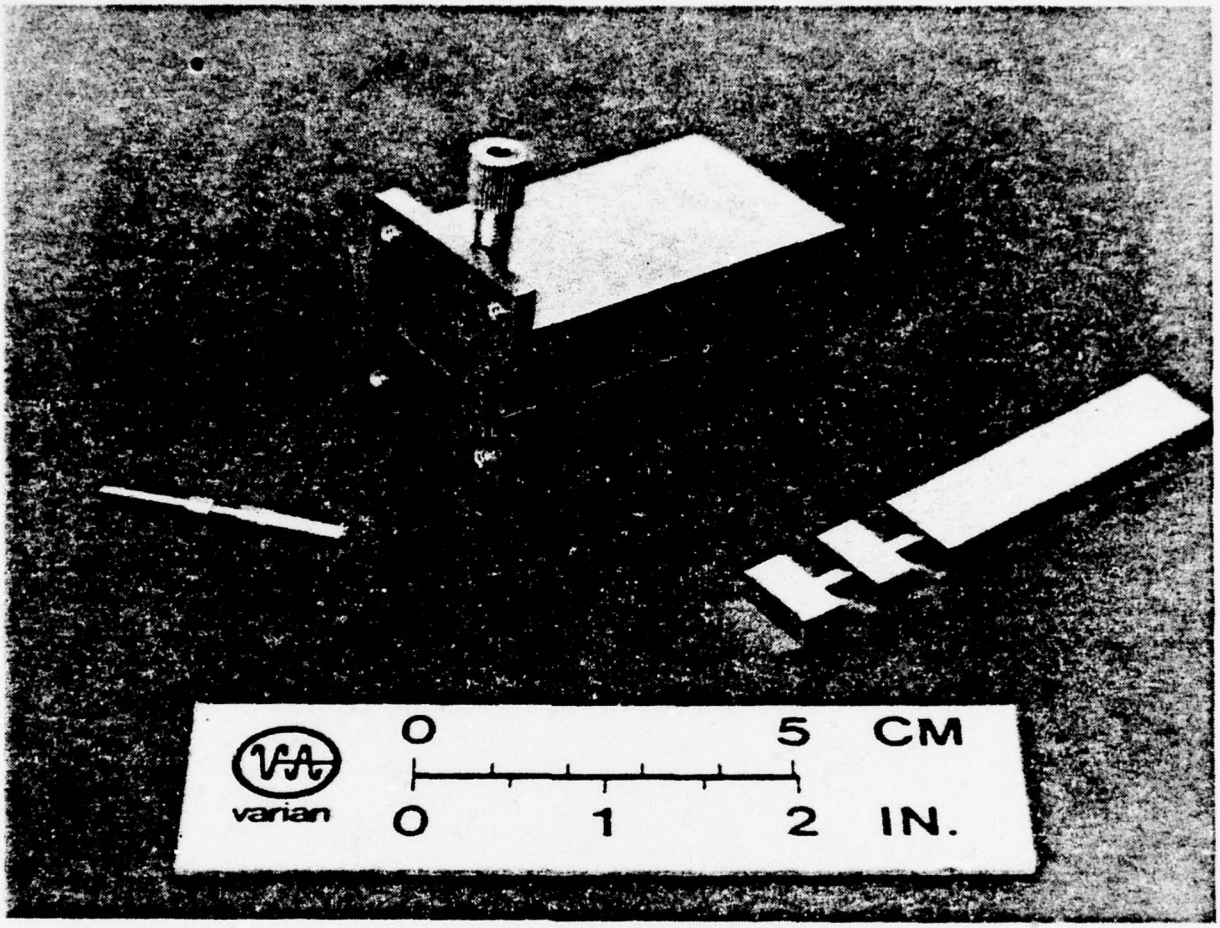


Figure 4.1. Ku-Band IMPATT Waveguide-Coaxial Test Circuit

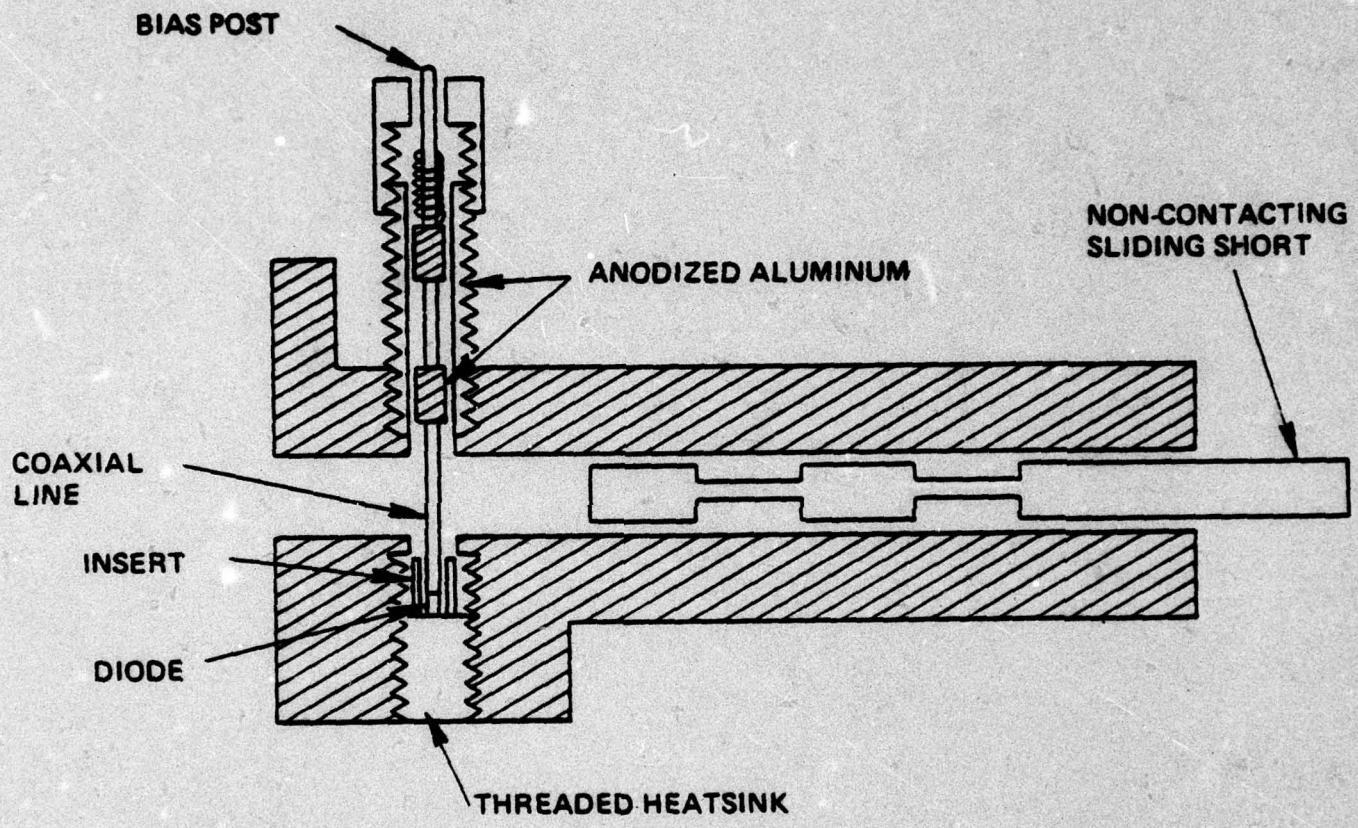


Figure 4.2 Ku-Band IMPATT Test Circuit

Other types of circuits, such as those using a "hat" resonator were not tried as they suffer from poor reproducibility and multi-mode operation. Also, it was felt that the coaxial-waveguide circuit was most useful in characterizing the devices since it is similar to most power combining circuits in which the diodes will probably be used.

An earlier version of this circuit was delivered to China Lake early in the program.

4.2 MODULATOR DEVELOPMENT

Since the diodes developed for this program were to operate at 125-nsec pulse lengths, a new modulator circuit was designed to have adequate rise times for these short pulse lengths. An outside consultant was retained to design and build a modulator capable of satisfying these requirements.

The final modulator design incorporates a commercially produced pulse generator with higher-power output stages. Siliconix VFETs were used on the output stage since they could handle the higher currents while still performing with adequate rise and fall times.

The modulator was designed to operate over a range of pulse lengths and duty cycles as it was felt this would be useful for a laboratory model. A shut-down circuit was designed to protect the output transistors in case of an IMPATT diode short. Also, a crowbar circuit was designed to protect the output transistors from over-voltage.

This modulator was also delivered to China Lake for evaluation as part of the contract requirements.

4.3 IMPEDANCE MEASUREMENTS

Pulsed impedance measurements were done during the program to aid in device, package and circuit design. On the basis of the impedance measurements, a circuit model was developed for the device and package combination.

Pulsed impedance measurements were done in a much less direct way than would be done for a conventional CW case. First, the diode is placed in the coaxial-waveguide circuit and tuned for maximum output power at some given frequency. This is schematically represented in Figure 4.3a. The diode and heat sink are removed from the circuit, and the reflection coefficient looking into the circuit is measured with the end of the coaxial line used as the reference plane as in Figure 4.3b. An SMA coaxial line, specially modified to be used as a probe, is used with a Hewlett-Packard network analyzer to measure the reflection coefficient. The large signal impedance of the diode is assumed to be the negative of the circuit impedance.

This type of impedance measurement has several drawbacks. First, it is difficult to measure the diode impedance as a function of frequency. The procedure is fairly time consuming for each diode. Also, since the real part of the diode impedance for large area pulsed devices is typically under 1 ohm, the overall accuracy of the measurement becomes doubtful. A load impedance under an ohm in a 50-ohm system corresponds to approximately 0.25 dB return loss. As a result, the measurement is very dependent on fixture losses and initial short calibration of the coaxial line.

Measured values of reactance are shown in Figure 4.4 for diodes of two different junction areas. These values represented the extremes of junction capacitances used for this program. The measured values were used with a diode model to aid in package and circuit design. The real part of the impedance fell into the range of -0.4 ohms to -1.5 ohms for power levels in the 7- to 9-watt range. There was not a clear correlation of negative resistance with frequency due to the inherent measurement errors.

4.4 DEVICE MODEL AND PACKAGE PARASITICS

Since the large reactance associated with the single-drift device in Ku-band was an important factor in limiting the peak powers, a model was used for the IMPATT chip based on measured impedance data to evaluate the effects of package parasitics. The model, developed by M.S. Gupta[28], is shown in Figure 4.5. It includes the junction capacitance, C, and avalanche inductance, L, while the

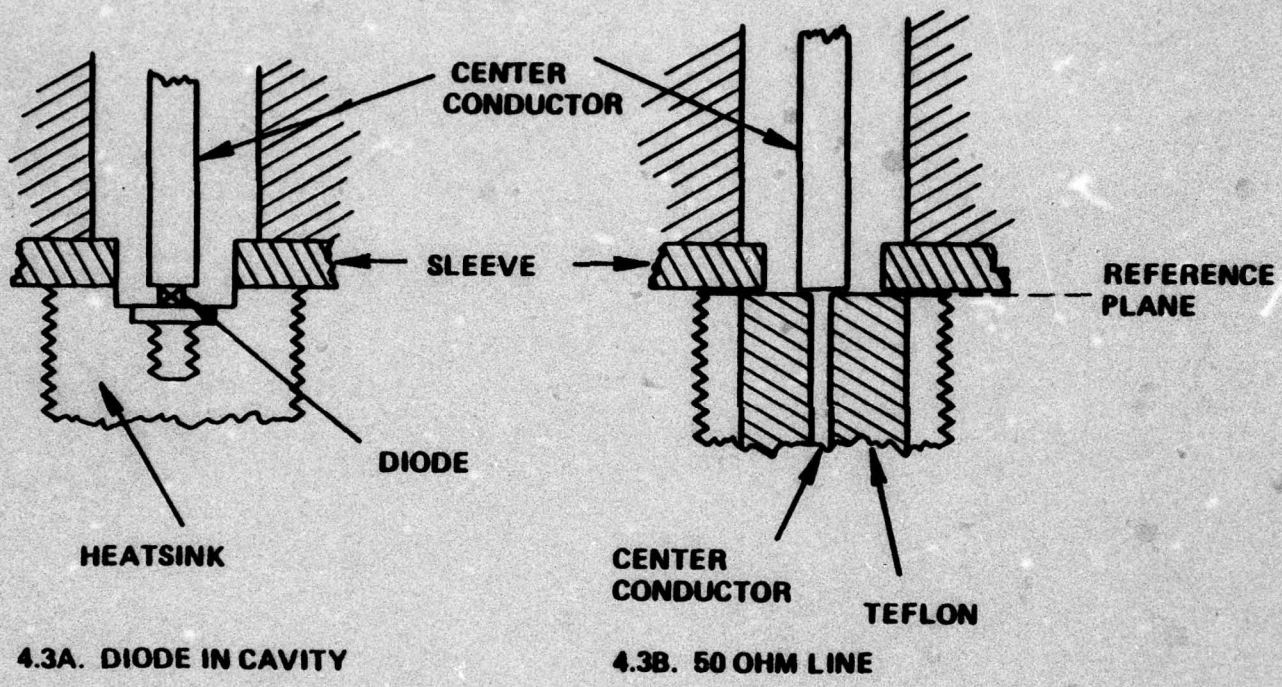


Figure 4.3 Pulsed IMPATT Impedance Measurement

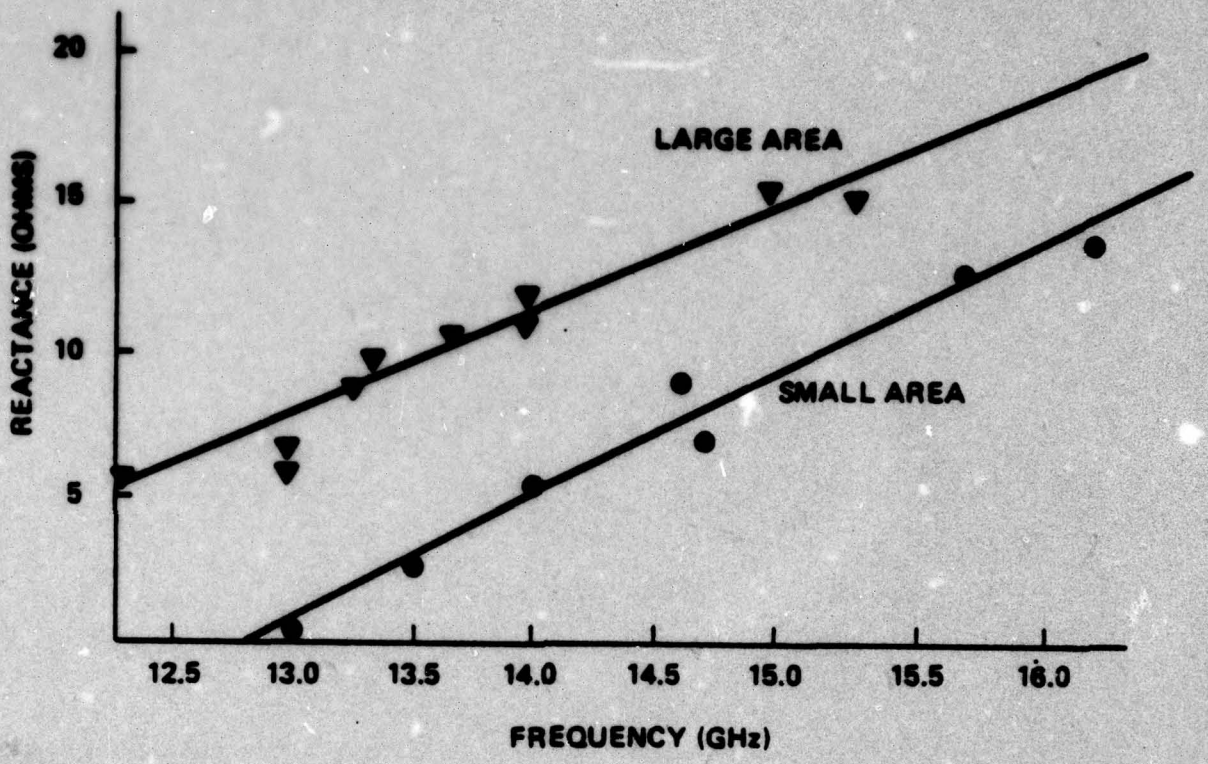


Figure 4.4 Pulsed Diode Reactance as a Function of Frequency for Diodes of Different Areas

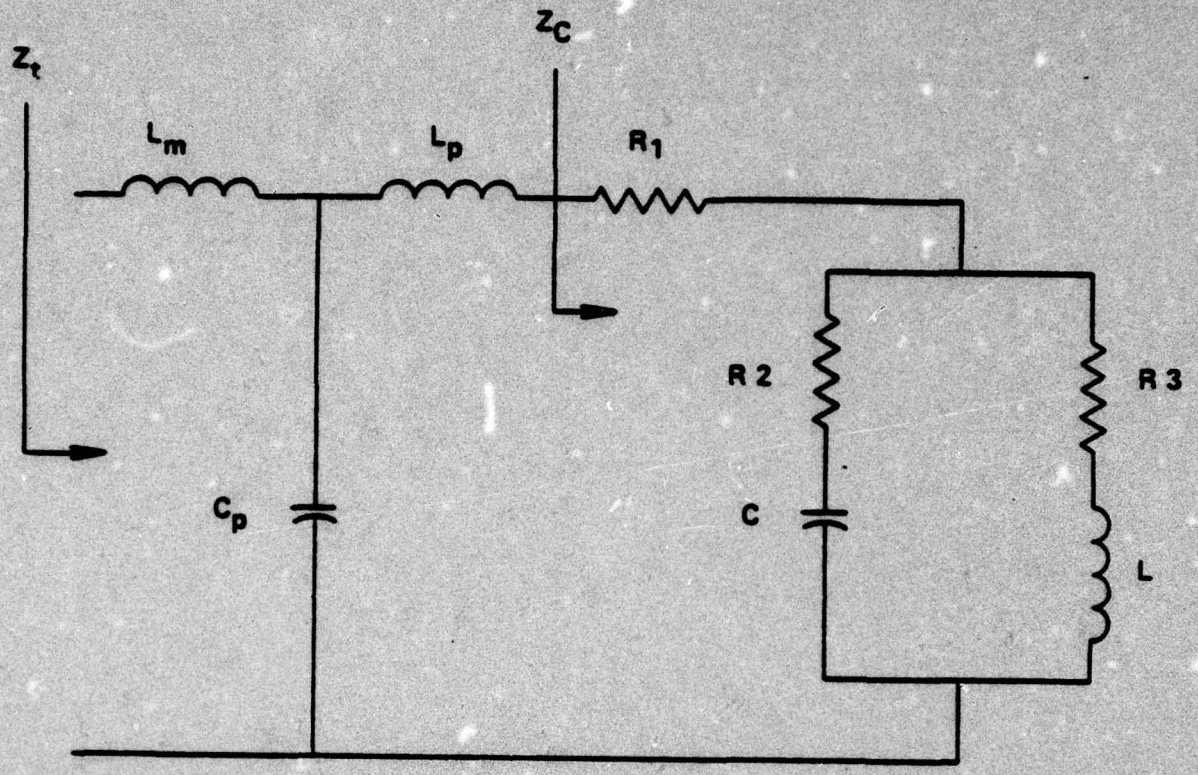


Figure 4.5 IMPATT Model Including Package Parasitics

values of resistance have little physical significance. The package parasitics are represented by the bondwire inductance, L_p; ceramic capacitance, C_p; and the inductance associated with the stored energy around the diode, L_m. It should be noted that the last term, L_m, is dependent on the fixture in which the diode impedance is measured.

Originally, the X-band IMPATTS were packaged with ribbon in the N-33 package as shown in Figure 4.6. The package parasitics are too high for Ku-band operation, so the N-57 package was used with crossed ribbon leads. Later, mesh bonding straps replaced the ribbon in an effort to reduce further the bond wire inductance, as seen in Figure 4.7. These package parasitics can be measured by CW means on an automatic network analyzer with a method described by Monroe[29] using open and shorted packages.

The IMPATT model was used initially to determine the effect the package parasitics had on terminal impedance. Figure 4.8 is a plot of the theoretical large signal impedance of a pulsed Ku-band IMPATT using various bondwire inductances. At 14 GHz, approximately 3.5 ohms of reactance are saved by using mesh bond straps. The values of the various elements of the model are summarized in Table 4.1.

4.5 OPTIMUM DIODE AREA

The peak pulsed powers obtained during this program were limited more by circuit matching limitation than thermal excesses. In the CW case, the power a diode can deliver is limited by the temperature rise of the junction. A pulsed diode, on the other hand, is usually used at a low enough duty cycle that the average power dissipated inside the diode is not enough to lead to excessive junction temperature. The peak power output increases with the junction area until some sort of circuit matching limitation is met.

Figures 4.9 and 4.10 show pulsed power and efficiency as a function of diode area for two duty cycles. The efficiency of the smaller area devices is limited by the intrinsic efficiency of the diode. As the junction area increases, the ability of the circuit to match the diode impedance decreases, causing the

Figure 4.6. N57 with Double Ribbon Bond Leads

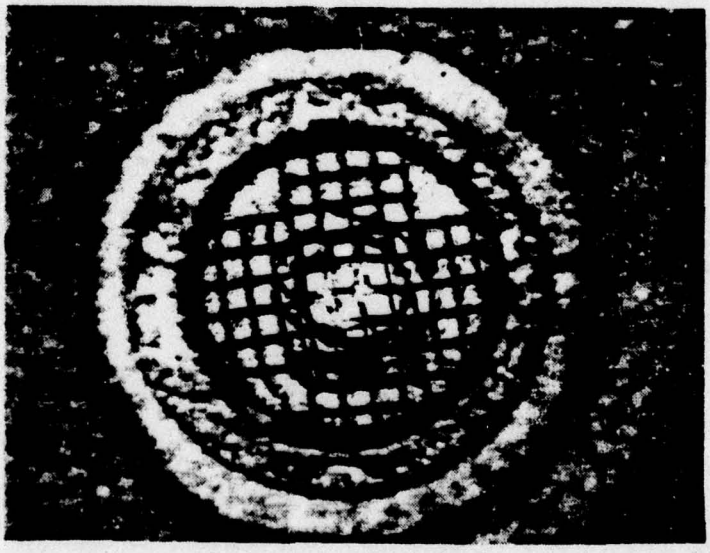


Figure 4.7. N57 with Double Mesh Bond Leads

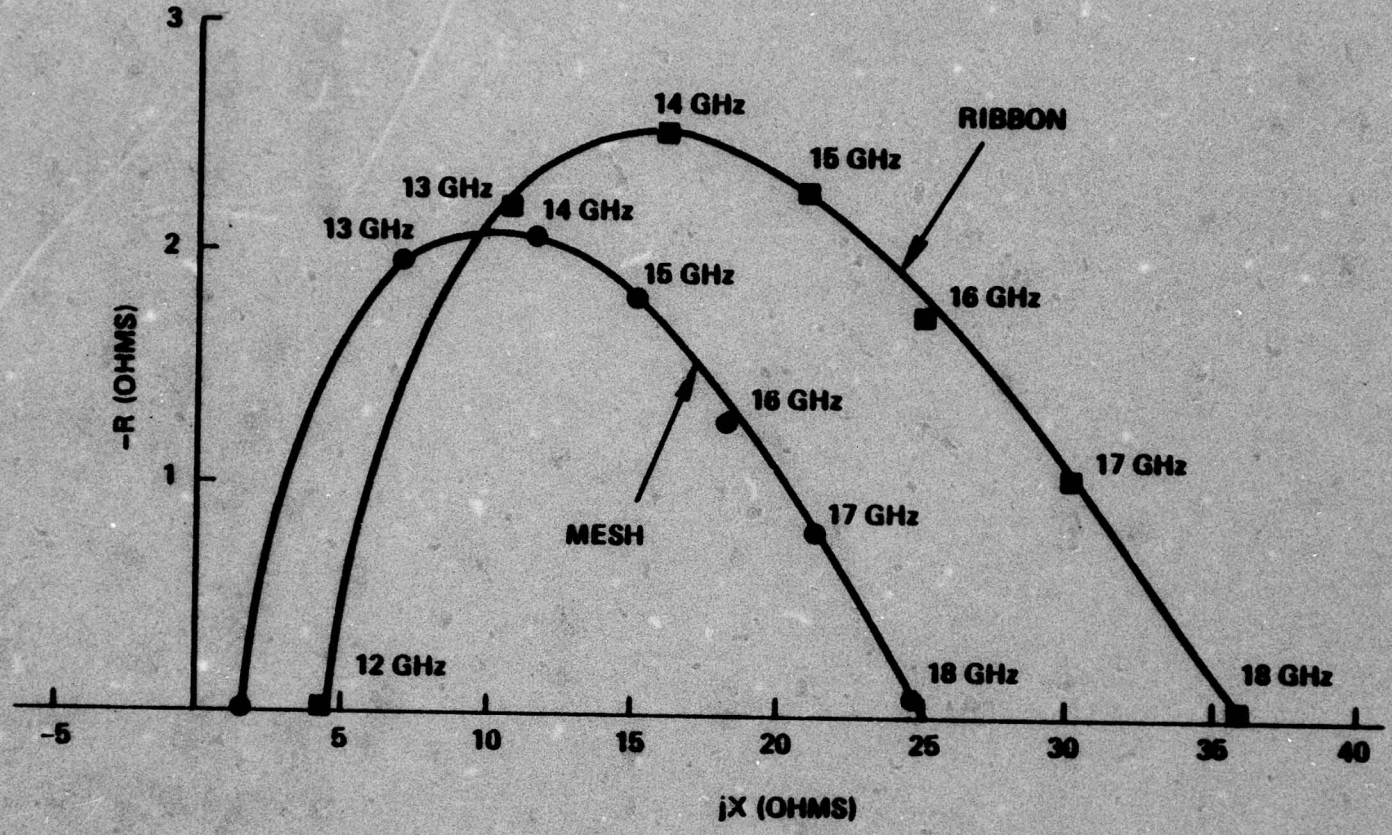


Figure 4.8 Impedance Calculated from Model Using Different Bondwire Inductances

TABLE 4.1
MODEL PARAMETERS FIT TO MEASURED DATA

	SMALL AREA DEVICE	LARGE AREA DEVICE
L (nh)	0.1	0.05
R_1 (Ω)	3.0	3.0
C (pf)	2.2	4.3
R_2 (Ω)	-2.0	4.3
R_3 (Ω)	4.0	-2.0
L_p (nh)	0.12	0.12
Cp (pf)	0.25	0.25
Lm (nh)	0.08	0.08

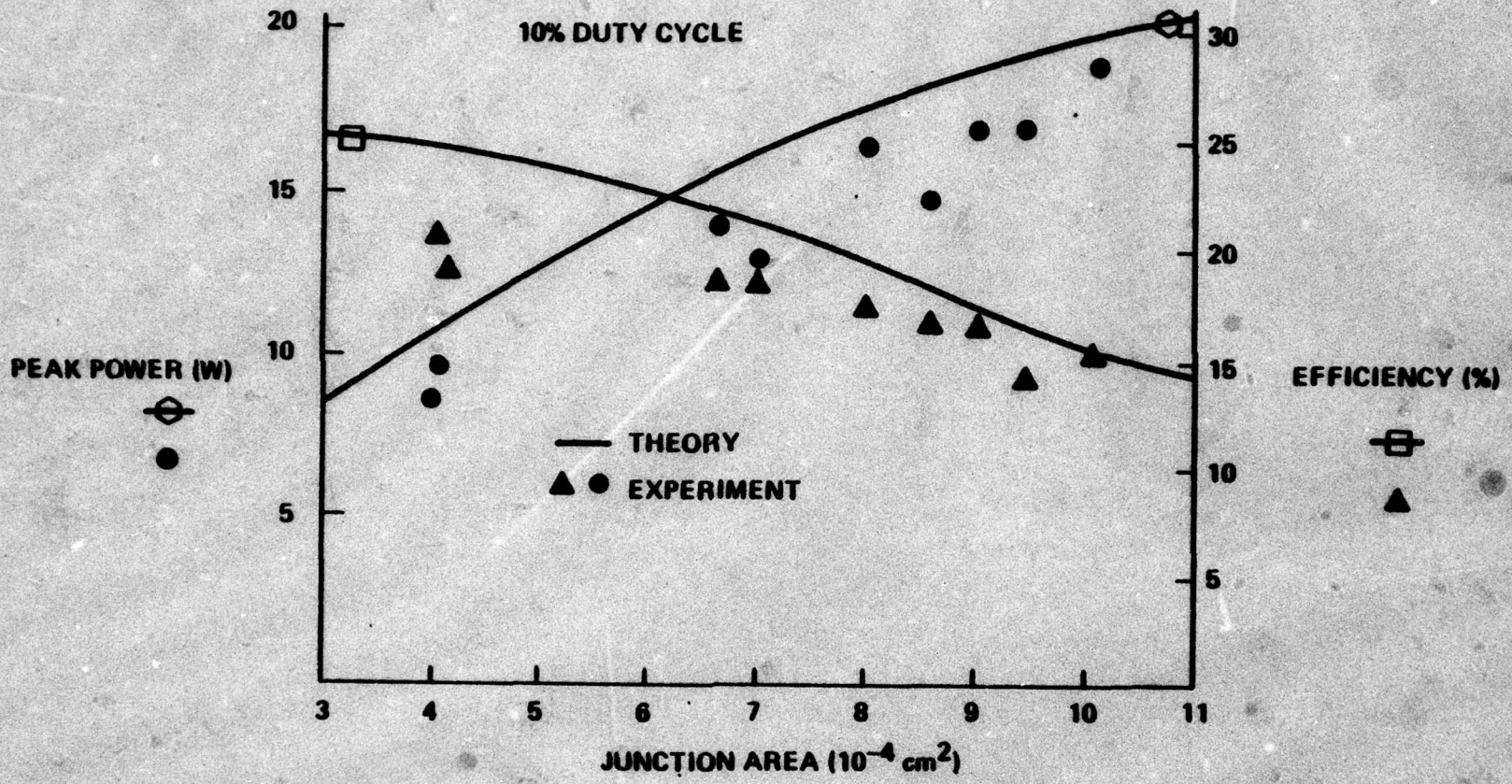


Figure 4.9. Theoretical and Experimental Power and Efficiency vs Junction Area for Wafer E442

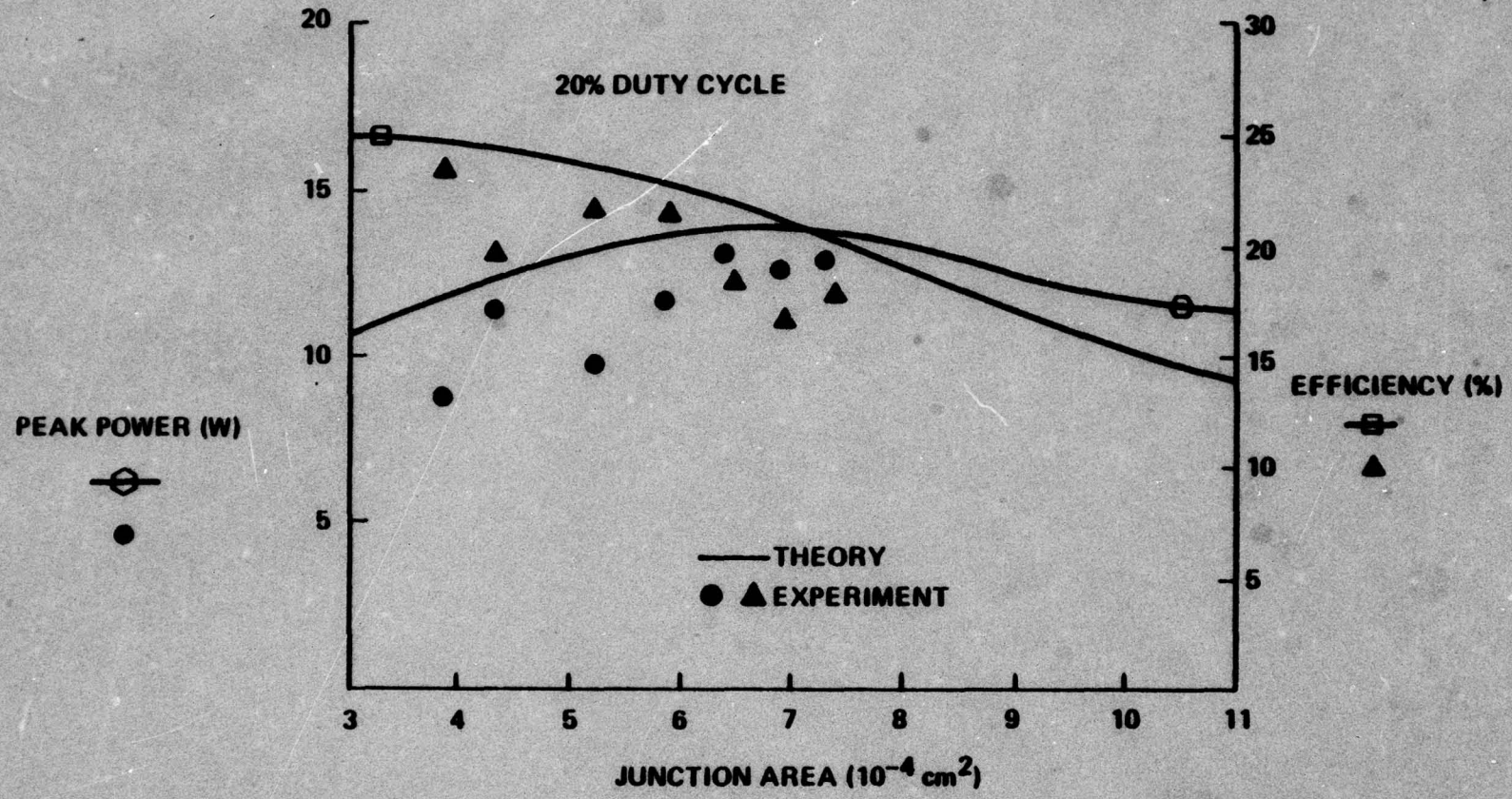


Figure 4.10 Theoretical and Experimental Power and Efficiency vs Junction Area for Wafer E442

effective diode efficiency to decrease. The power no longer increases linearly with the area as seen in these examples.

Although the situation is very complicated, due to the interdependence of the variables, it is possible to describe qualitatively the dependence of microwave power output and efficiency on diode area in an analytic manner. The analysis proceeds as follows: The rf power output is given by:

$$P_{out} = 1/2\ (|G| - G_{sh})\ V_1^2 \tag{1}$$

where G is the large signal negative conductance of the diode and the G_{sh} is the shunt loss to the diode and circuit. V_1 is the applied rf voltage. The dependence of the large signal negative conductance upon rf voltage may be approximated by a high order polynominal of the form given by Dalman, et al[30].

$$G = G_{ss}\ (1 - g_1 \alpha^2 + g_2 \alpha^3) \tag{2}$$

where G_{ss} is the small signal (maximum) negative conductance of the diode, α is the modulation depth = V_1/V_o, where V_o is the dc operating voltage. The g_i's are coefficients of the expansion, which may be determined by fitting the above expression to experimental data, for example, or to a theoretical curve.

In order to obtain an analytically tractable solution, only the first two terms of (2) are employed. Equation (2) is substituted into (1). The result is differentiated with respect to V_1 in order to determine the rf voltage which optimizes the output power:

$$V_{1,\,opt} = \frac{V_o}{\sqrt{2g1}} \left[1 - \frac{G_{sh}}{G_{ss}}\right]^{1/2} \tag{3}$$

This value of $V_{1,opt}$ is then substituted back into (1), in order to determine the optimum output power:

$$P_{out,\,opt} = \frac{V_o^2}{8g_1} G_{ss} \left[1 - \frac{G_{sh}}{G_{ss}}\right]^2 \tag{4}$$

Clearly in the absence of any shunt losses ($G_{sh} = 0$), the maximum output power is given by:

$$P_{max} = \frac{V_o^2}{8g_1} G_{ss} \tag{5}$$

The ratio of P_{opt}/P_{max} defines the "diode/circuit transmission efficiency" n_{trans}:

$$n_{trans} = \left[1 - \frac{G_{sh}}{G_{ss}}\right]^2 \tag{6}$$

The problem is now reduced to relating G_{ss}, G_{sh}, and the intrinsic efficiency of the diode to the diode area, A.

The intrinsic power-generating capability of the diode is related to its intrinsic efficiency by the following well known expression:

$$P_o = \frac{n_o}{1-n_o} \frac{\Delta T}{\theta} \tag{7}$$

where n_o is the intrinsic diode efficiency, ΔT is the temperature rise due to dc dissipation, and θ is the thermal resistance of diode and heat sink. This thermal resistance may be expressed in terms of the diameter, d, of the junction as:

$$\theta = \frac{1}{2\sigma_{hs}d} + \frac{4t}{\pi d^2 \sigma_{GaAs}} \tag{8}$$

where the first term is due to the spreading resistance of the heat sink and the second term is due to the separation of the heat-generating plane from the heat sink. Since the first term usually dominates for larger junction diameters, the thermal resistance is approximately given by:

$$\theta \simeq \frac{1}{2\sigma_{hs}d} \tag{9}$$

(where σ_{hs} = 3W/cm/^oC for gold). The dc input power to the diode is given by the product of dc operating voltage, V_o, and dc operating current, J_o, and area, A

$$P_{dc} = V_o J_o A = V_o I_o \tag{10}$$

The operating voltage, V_o, is also dependent upon both T and $J_o A$ according to:

$$V_o = V_{BR}\ (T) + I_o R_{sc} \tag{11}$$

where V_{BR} is the breakdown voltage, and R_{sc} is the space charge resistance. It is necessary to assume that for a given temperature rise, ΔT, V_o is approximately constant (i.e., neglect space charge contribution), which is a good

approximation based on experimental data. (Note: V_o is also dependent upon V_1, but a constant voltage supply is assumed.) Thus, the dc input power is approximately given by:

$$P_{dc} \simeq \Delta T\,(2\alpha d) = V_o J_o A \tag{12}$$

and, the operating current density J_o may be written as:

$$J_o = \frac{\Delta T(2\alpha d)}{V_o A} \text{ where } A = \frac{\pi d^2}{4}$$

$$J_o = \frac{8\alpha\Delta T}{\pi V_o d} \tag{13}$$

According to R. L. Kuvas[31], the intrinsic conversion efficiency of an "ideal" Read diode may be written as:

$$n_o = h_1 k_1 \frac{V_1}{V_o}(1-B_1) \tag{14}$$

where h_1 is the well known drift region transport factor:

$$h_1 = \frac{1-\cos\psi}{\psi}\left[\frac{\ell_d}{W}\right] \tag{15}$$

ψ is the transit angle; ℓ_d is the length of the drift zone; W is the total depletion width, k_1 is the ratio of two modified Bessel functions:

$$k_1 = \frac{Q_1\,(2D_1)}{Q_o\,(2D_1)} \tag{16}$$

which are dependent upon the rf voltage, V_1 through the normalized field parameter D_1:

$$D_1 = \frac{|a_1| \; V_1}{\omega_0 W} \tag{17}$$

Here, $|a_1|$ is related to the field derivative of the ionization rates and ω_0 is the angular frequency.

B_1 is the large signal avalanche resonance factor, which is also dependent upon the rf voltage:

$$\begin{aligned} B_1 &= \frac{|a_1| \; J_0}{\epsilon \omega_0^2} \left(\frac{2k_1}{D_1} \right) \\ &= \frac{|a_1| \; J_0}{\epsilon \omega_0 2} \left(\frac{2k_1 W \omega_0}{|a_1| \; V_1} \right) \\ &= \frac{2k_1 J_0 W}{\epsilon \omega_0 V_1} \end{aligned} \tag{18}$$

where ϵ is the dielectric permittivity of GaAs.

B_1 may be rewritten in terms of the expression previously derived for J_0, equation (13):

$$B_1 = \frac{2k_1 (8\sigma\Delta T)W}{(\pi V_o d)\ \epsilon\omega_o V_1} = \frac{16k_1\sigma\ \Delta TW}{\pi d V_o\ \epsilon\omega_o V_1} \tag{19}$$

In order to simplify the analysis, it is assumed W is not a function of drive or temperature which is consistent with the assumption that V_o is quasi-static. This implies that the transport factor h_1 is also quasistatic with respect to any change in area for fixed ΔT. In order to be consistent with the analysis employed to derive the optimum rf voltage for maximum output power, the optimum rf voltage expression (3) should be substituted for V_1 wherever it appears in the intrinsic diode efficiency expression (14). Thus, (14) reduces to the following lengthy expression:

$$n_o = h_1 k_1 \frac{\left(1 - \frac{G_{sh}}{G_{ss}}\right)^{1/2}}{\sqrt{2\ g_1}} \left[1 - \frac{16k_1\sigma\Delta TW\ \sqrt{2a_1}}{\pi d V_o^{\,2}\ \epsilon\omega_o}\right. \left.\times \left(1 - \frac{G_{sh}}{G_{ss}}\right)^{-1/2}\right] \tag{20}$$

The expression for the experimentally measured output power is given by the product of the intrinsic diode output power, P_o and the transmission efficiency, n_{trans}:

$$P_{out} = n_{trans} \; P_o$$

$$= n_{trans} \frac{n_o}{1 - no} \; (\Delta T) \; (2\sigma d) \tag{21}$$

The remaining problem is to relate the ratio G_{sh}/G_{ss} to the physical parameters of the diode and circuit. This has been done by Kondo, et al[32]. The shunt loss is merely given as:

$$G_{sh} = \omega_o^2 C_o^2 R_s A^2 \tag{22}$$

where C_o is the diode capacitance/unit area and Rs are the series loss due to the diode and circuit. The ratio, $g = G_{sh}/G_{ss}$ is then given by:

$$g = \frac{\omega_o^2 C_o^2 R_s \left(\frac{\pi d^2}{4}\right)^2}{\frac{\partial G_{sso}}{\partial J_o}\left(\frac{2\sigma\Delta T}{V_o}\right) d} \tag{23}$$

where G_{ss} is the small signal (max) negative conductance per unit area. The expression for g may be re-written in a more convenient form containing only the dependence on junction diameter:

$$g = \left(\frac{d}{d_o}\right)^3$$

(24)

$$\text{where} \qquad d_o^{\,3} = \left(\frac{4}{\pi}\right)^2 \frac{\dfrac{\partial G_{sso}}{\partial J_o}\left(\dfrac{2\sigma}{V_o}\right)}{\omega_o^{\,2} C_o^{\,2} R_s}\,\Delta T$$

is taken to be a constant in this analysis.

An analytic expression can be written down and evaluated for the term $\partial G_{sso}/\partial J_o$, however, it is very complicated. The assumption made here is that to first order the dependence is linear; although in a "Read" diode, it is somewhat sublinear.

Before proceeding further, it is worthwhile to examine qualitatively the expressions which have been derived, so that one does not miss the "forest" for all of the "trees". Re-writing equation (21), emphasizing the terms containing the diameter:

$$P_o = \frac{k_1\left[1-\left(\dfrac{d}{d_o}\right)^3\right]^{5/2}\left\{1-\dfrac{k_1\cdot(\text{const.})_1}{d\left[1-\left(\dfrac{d}{d_o}\right)^3\right]^{1/2}}\right\} d\cdot(\text{const.})_2}{1-\left\{k_1\left[1-\left(\dfrac{d}{d_o}\right)^3\right]^{1/2}\cdot(\text{const.})_3\cdot\left(1-\dfrac{k_1\,(\text{const.})_1}{d\left[1-\left(\dfrac{d}{d_o}\right)^3\right]^{1/2}}\right)\right\}} \tag{25}$$

where

$$(\text{const.})_1 = \frac{16\sigma\Delta T W\sqrt{2g_1}}{\pi V_o^2 \omega_o}$$

$$(\text{const.})_2 = \left(\frac{h_1}{\sqrt{2g_1}}\right)(\Delta T)(2\sigma)$$

$$(\text{const.})_3 = \frac{h_1}{\sqrt{2g_1}}$$

where

$$k_1 = \frac{Q_1\left\{\frac{2|a_1|}{\omega_o W}\frac{V_o}{\sqrt{2g_1}}\left[1-\left(\frac{d}{d_o}\right)^3\right]^{1/2}\right\}}{Q_0\left\{\frac{2|a_1|}{\omega_o W}\frac{V_o}{\sqrt{2g_1}}\left[1-\left(\frac{d}{d_o}\right)^3\right]^{1/2}\right\}}$$

k_1 is not a strong function of V_1, so to a good approximation $k_1 \simeq 0.86$, although, k_1 will decrease with increasing d thus decreasing the intrinsic efficiency of the diode.

For fixed T, increasing d increases the input power. This directly increases P_{out}. However, increasing d also decreases the transmission efficiency. So, it is immediately obvious there is an optimum d for maximum P_{out}. On the other hand, the increase in input power increases the intrinsic efficiency while the decrease in rf voltage decreases the intrinsic efficiency. Thus, there will be a peak in n_o. Although it is not immediately obvious, it is probable that there will be a peak in efficiency at a smaller value of d than required for maximum P_{out}.

In spite of the rather gross assumptions made throughout this analysis, the theoretical predictions are in good qualitative agreement with experimental results.

The important feature of the analysis is the parameter "do". Clearly by increasing "do", such as by reducing the series losses contained in R_s, or by going to a double-drift structure in which the depletion width W is larger, hence Co is smaller, greater power may be realized in larger area devices. This is what is intuitively expected.

The analysis may be extended to illustrate the dependence of P_{out} and efficiency on temperature rise (ΔT) which is dependent, of course, on the duty cycle of the pulse, for a given (constant) junction area.

Thus, the analysis appears to provide a useful guideline for predicting the performance of structures not realized to date.

5. CONCLUSIONS

5.1 MATERIAL GROWTH

During the nine-month time interval, both LPE and VPE growth techniques were employed to produce Ku-band pulsed Read type IMPATT wafers. The LPE technique was focused on hi-lo Read designs using a p^+ grown junction. Initial work with Schottky barriers as well as Schottky barrier work done on an earlier program for the Air Force indicated a direct comparison of Schottky barrier versus a grown junction was more difficult than initially anticipated. This was due to the fact that the p^+ growth removed part of the n^+ epitaxial layer making the comparison invalid.

The vapor-phase approach initially concentrated on lo-hi-lo modified Read profiles using a Schottky barrier. Difficulties in growing a "good" profile prevented us from obtaining rf results comparable to the LPE hi-lo devices. While the lo-hi-lo design should be slightly more efficient than the hi-lo profile, it proved to be much harder to grow due to the greater sensitivity to avalanche width. While the lo-hi-lo wafers did not provide superior rf performance, much was learned concerning Schottky barrier metallizations and device reliability.

The remainder of the VPE work centered on grown junction hi-lo wafers. The reactor had been modified to grow highly doped p-material using cadmium for the contact. The hi-lo profile was chosen in the interest of time since we had much more experience with this profile based on our work in LPE. This removed one more variable and allowed a fair comparison of liquid- and vapor-phase epitaxy.

5.2 DEVICE DESIGN

During this study, theoretical computer programs were established which accurately predict static field and small signal characteristics for hi-lo and lo-hi-lo devices. Very good agreement between calculated and experimental

operating voltages, frequency and efficiency were achieved when the actual measured device doping profile was employed in the calculation.

The best rf performances were obtained with p^+-hi-lo structures. The doping profile specifications which provide the best results and are theoretically optimum for the pulsed hi-lo devices are summarized in Table 5.1. Peak power of 16 W with 19% efficiency was obtained at 14 GHz. Efficiencies of over 24% were obtained with smaller area devices.

Comparison of Schottky barrier and grown junction diodes was done on the basis of rf performance, reliability, and thermal resistance. While the best rf performances were obtained with grown junction devices, this is due to the fact that a greater number of grown junction wafers were fabricated. We would expect comparable rf performance to be obtained with Schottky barrier devices. The reliability of the Schottky barrier devices was clearly inferior to the grown junction devices. A Pt-Ti:W-Au metallization was found to be more stable than either Au or Pt systems. The thermal resistance of the Schottky barrier diodes was typically $0.5^{\circ}C/W$ better than the grown junction version. The contribution of the 1 μm p^+ layer to the total device thermal resistances is not really significant for the large area pulsed devices.

5.3 CIRCUIT DESIGN AND DEVICE EVALUATION

A versatile coaxial-waveguide hybrid circuit was designed for Ku-band which was capable of matching over a wide range of real and imaginary parts. The circuit is similar to typically used power combiner configurations and therefore provides a good basis for diode selection. It provided repeatable operation without problems with multi-mode operation.

The impedance of the device at 14 GHz was obtained from measuring the circuit impedance with a probe on a network analyzer. The negative real part proved very difficult to measure in this 50-Ω system since it was usually less than 1 ohm for the large area devices. The reactive component at 14 GHz was in the 10-15 Ω range including the mount inductance associated with the circuit. Significant reduction of overall reactance was obtained by employing mesh bond

TABLE 5.1
OPTIMUM DOPING PARAMETERS FOR Ku-BAND PULSED IMPATT

AVALANCHE REGION		DRIFT REGION	
DOPING	LENGTH	DOPING	LENGTH
$7-10 \times 10^{16}$ cm^{-3}	0.23–0.35 μm*	$7-9 \times 10^{15}$ cm^{3}	3.5–4.0 μm

*Very critical

straps instead of the normally used ribbon in the packages. This allowed the circuit to more efficiently match larger area devices to obtain higher peak powers.

Finally, based on the impedance levels and the efficiency versus area characteristics determined for 14 GHz single drift pulsed Read devices, performance is being limited by impedance matching and hence circuit losses. Higher powers can be obtained by improving the device profile for higher overall conversion effiencies or higher current density operation. A significant improvement in power and upper frequency limitations can be anticipated for double-drift GaAs pulsed devices since the impedance limitation with occur for larger area devices.

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